



STM32F103x6 STM32F103x8 STM32F103xB

Performance line, ARM-based 32-bit MCU with Flash, USB, CAN
7 timers, 2 ADC, 9 communication interfaces

Preliminary Data

Features

■ Core

- ARM 32-bit Cortex-M3™ CPU
- 72 MHz, 90 DMips with 1.25 DMips/MHz
- Single-cycle multiplication and hardware division for computational acceleration

■ Memories

- From 32 Kbytes to 128 Kbytes Flash program memory
- From 6 Kbytes to 20 Kbytes SRAM
- Multi-boot capability

■ Clock, Reset and Supply Management

- 2.0 to 3.6V application supply and I/Os
- Internal regulator for core supply
- Embedded high-speed quartz oscillator from 4 to 16 MHz
- Power on / power down reset (POR/PDR), programmable voltage detector (PVD), brown-out detector
- Embedded RTC oscillator running from external 32 kHz crystal
- Embedded internal RC running at 8 MHz
- Embedded internal RC running at 32 kHz
- Embedded PLL for CPU clock
- Real-Time Clock with calibration capability for precise clock-calendar function

■ Low Power

- 4 power saving modes: 2 SLEEP, STOP and STANDBY modes
- VBAT supply for RTC and backup registers

■ Nested Interrupt Controller

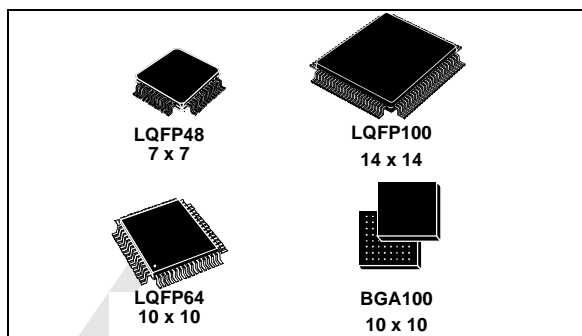
- Superior multiple vector interrupt handling
- 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M3)
- Very low latency interrupt processing down to 6 CPU cycles with tail-chaining

■ 2 x 12-bit A/D Converters (16-channel)

- Sampling frequency up to 1 MHz
- Conversion range: 0 to 3.6 V
- Dual-sample and hold capability
- Auto-calibration
- Synchronizable with advanced control timer
- Temperature sensor

■ Debug Mode

- Serial wire debug (SWD) and JTAG interfaces
- Serial wire viewer
- 8 hardware breakpoints



■ Up to 80 Fast I/O Ports

- 32/49/80 multifunctional bidirectional 5V-tolerant I/Os
- All mappable on 16 external interrupts
- Up to 80 ports with external interrupt capability
- Possibility of locking the I/O in chosen alternate function configuration
- I/Os on APB2 with up to 18 MHz toggling speed
- Atomic read/modify/write operations

■ Up to 7 Timers

- Up to 3 synchronizable 16-bit timers, each with up to 4 channels used for input captures/output compares, PWM or pulse counter
- 16-bit 6-channel advanced control timer, configurable with up to 4 channels for input capture or output compare
 - Ideal for induction/brushless DC motors
 - Up to 6 channels for PWM output
 - Dead time generation, edge/center-aligned waveforms and emergency stop
 - Emergency stop input with possibility of locking the state of the PWM outputs
- 2 x 16-bit watchdog timers (Independent and Window)
 - Independent watchdog running on its own protected clock system
- SysTick timer: a 24-bit down counter with auto reload capability with programmable clock source for timebase functions

■ Up to 9 Communication Interfaces

- Up to 2 x I²C interfaces (SMBus/PMBus)
- Up to 3 USARTs asynchronous serial interfaces (4.5 MBit/s) providing:
 - Smart Card ISO7816 interface, LIN master slave capability, IrDA capability, Modem control
- Up to 2 SPI synchronous serial interfaces (18 Mbit/s)
- CAN interface (2.0B Active)
- USB 2.0 full speed interface

Note: Please refer to [Table 1](#) for a comprehensive list of available features per device.

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Contents

- 1 Introduction 6**
- 2 Description 6**
 - 2.1 Device summary 7
 - 2.2 Overview 8
- 3 Pin Descriptions 14**
- 4 Memory Mapping 20**
- 5 Electrical characteristics 21**
 - 5.1 Test conditions 21
 - 5.1.1 Minimum and maximum values 21
 - 5.1.2 Typical values 21
 - 5.1.3 Typical curves 21
 - 5.1.4 Loading capacitor 21
 - 5.1.5 Pin input voltage 21
 - 5.1.6 Power supply scheme 22
 - 5.1.7 Current consumption measurement 23
 - 5.2 Absolute maximum ratings 24
 - 5.3 Operating conditions 26
 - 5.3.1 General operating conditions 26
 - 5.3.2 Operating conditions at power-up / power-down 26
 - 5.3.3 Embedded reset and power control block characteristics 27
 - 5.3.4 Embedded reference voltage 27
 - 5.3.5 Supply current characteristics 28
 - 5.3.6 External clock source characteristics 33
 - 5.3.7 Internal Clock source characteristics 37
 - 5.3.8 PLL characteristics 38
 - 5.3.9 Memory characteristics 39
 - 5.3.10 EMC characteristics 40
 - 5.3.11 Absolute Maximum Ratings (Electrical Sensitivity) 41
 - 5.3.12 I/O port pin characteristics 43
 - 5.3.13 NRST pin characteristics 48

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	5.3.14	TIM timer characteristics	49
	5.3.15	Communications interfaces	49
	5.3.16	CAN - Controller Area Network Interface	56
	5.3.17	12-bit ADC characteristics	56
	5.3.18	Temperature sensor characteristics	58
6		Package characteristics	59
	6.1	Package Mechanical Data	59
	6.2	Thermal characteristics	62
7		Order codes	63
	7.1	Future family enhancements	63
8		Revision history	64

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List of tables

Table 1.	Device features and peripheral counts (STM32F103 Performance Line)	7
Table 2.	Pin Definitions	16
Table 3.	Voltage characteristics	24
Table 4.	Current characteristics	24
Table 5.	Thermal characteristics	25
Table 6.	General operating conditions	26
Table 7.	Operating conditions at power-up / power-down	26
Table 8.	Embedded reset and power control block characteristics	27
Table 9.	Embedded bandgap reference voltage	27
Table 10.	Maximum current consumption in RUN and SLEEP modes	28
Table 11.	Maximum current consumption in STOP and STANDBY modes	29
Table 12.	Typical current consumption in RUN and SLEEP modes	30
Table 13.	Typical current consumption in STOP and STANDBY modes	31
Table 14.	Peripheral current consumption	32
Table 15.	High-speed external (HSE) user clock characteristics	33
Table 16.	Low-speed external user clock characteristics	33
Table 17.	HSE 4-16 MHz oscillator characteristics	35
Table 18.	LSE oscillator characteristics (fLSE= 32.768 kHz)	36
Table 19.	HSI oscillator characteristics	37
Table 20.	LSI oscillator characteristics	37
Table 21.	Low-power mode wake-up timings	38
Table 22.	PLL characteristics	38
Table 23.	Flash memory characteristics	39
Table 24.	Flash endurance and data retention	39
Table 25.	EMS characteristics	40
Table 26.	EMI data	41
Table 27.	ESD absolute maximum ratings	41
Table 28.	Electrical sensitivities	42
Table 29.	I/O static characteristics	43
Table 30.	Output voltage characteristics (2.7 V < VDD < 3.6 V)	45
Table 31.	I/O AC characteristics for VDD= 2.7 to 3.6V	47
Table 32.	NRST pin characteristics	48
Table 33.	TIM characteristics	49
Table 34.	I2C Characteristics	50
Table 35.	SCL frequency table (fPCLKx=10 MHz., VDD = 3.3 V)	51
Table 36.	SPI characteristics	52
Table 37.	USB DC electrical characteristics	55
Table 38.	USB: Full speed electrical characteristics	55
Table 39.	ADC characteristics	56
Table 40.	ADC accuracy with fPCLK2 = 10MHz, fADC=10MHz, RAIN < 10kΩ, VDDA=3.3V	57
Table 41.	TS characteristics	58
Table 42.	Thermal characteristics	62
Table 43.	Order codes	63
Table 44.	Document revision history	64

List of figures

Figure 1.	STM32F103 Performance Line Block Diagram	13
Figure 2.	STM32F103 Performance Line LQFP100 Pinout	14
Figure 3.	STM32F103 Performance Line LQFP64 Pinout	14
Figure 4.	STM32F103 Performance Line LQFP48 Pinout	15
Figure 5.	Memory Map	20
Figure 6.	Pin loading conditions	22
Figure 7.	Pin input voltage	22
Figure 8.	Power supply scheme	22
Figure 9.	Current consumption measurement scheme	23
Figure 10.	RUN mode current consumption versus frequency (PLL off from 4 to 16 MHz at 3.3 V and 25 °C, 85 °C and 105 °C)	28
Figure 11.	RUN mode current consumption versus frequency (from 16 to 72 MHz at 3.3 V and 25 °C, 85 °C and 105 °C)	28
Figure 12.	Current consumption in STOP mode with regulator in Run Mode (at VDD = 3.3 V, 2.4 V and 2.0 V) versus temperature (-40 to 105 °C)	29
Figure 13.	Current consumption in STOP mode with regulator in Low Power mode (at VDD = 3.3 V, 2.4 V and 2.0 V) versus temperature (-40 to 105°C)	29
Figure 14.	Current consumption in STANDBY mode (at VDD = 3.3 V, 2.4 V and 2.0 V) versus temperature (-40 to 105 °C)	29
Figure 15.	VBAT Backup domain consumption (at VBAT = 3.3 V, 2.4 V and 1.8 V) versus temperature (-40 to 105 °C)	29
Figure 16.	High-speed external clock source AC timing diagram	34
Figure 17.	Low-speed external clock source AC timing diagram	34
Figure 18.	Typical application with a 8-MHz Crystal	35
Figure 19.	Typical application with a 32.768 kHz crystal	36
Figure 20.	RPU vs. VDD with VIN=VSS	44
Figure 21.	RPD vs. VDD with VIN=VDD	44
Figure 22.	Unused I/O pin connection	44
Figure 23.	Typical VOL and VOH at VDD=3.3V	45
Figure 24.	Typical VOL vs. VDD	46
Figure 25.	Typical VOH vs. VDD	46
Figure 26.	I/O AC characteristics definition	47
Figure 27.	Recommended NRST pin protection	48
Figure 28.	I2C bus AC waveforms and measurement circuit (to be split)	51
Figure 29.	SPI timing diagram - slave mode and CPHA=0	53
Figure 30.	SPI timing diagram - slave mode and CPHA=11)	53
Figure 31.	SPI timing diagram - master mode	54
Figure 32.	USB timings: definition of data signal rise and fall time	55
Figure 33.	ADC accuracy characteristics	57
Figure 34.	Typical connection diagram using the ADC	57
Figure 35.	Power supply and reference decoupling (VREF+ not connected to VDDA)	58
Figure 36.	Power supply and reference decoupling (VREF+ connected to VDDA)	58
Figure 37.	100-Low Profile Fine Pitch Ball Grid Array Package	59
Figure 38.	Recommended PCB Design rules (0.80/0.75mm pitch BGA)	60
Figure 39.	100-Pin Low-profile Quad Flat Package	60
Figure 40.	64-Pin Low-profile Quad Flat Package	60
Figure 41.	48-Pin Low-profile Quad Flat Package	61

1 Introduction

This databrief provides the STM32F103 Performance Line Ordering Information and Mechanical Device Characteristics.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10x Flash Programming Reference Manual*

For information on the Cortex-M3 core please refer to the Cortex-M3 Technical Reference Manual.

2 Description

The STM32F103 Performance Line family incorporates the high-performance ARM Cortex-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 128Kbytes and SRAM up to 20 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose timers with PWM outputs, as well as standard and advanced communication interfaces: up to two I²Cs and SPIs, three USARTs, an USB and a CAN.

The STM32F103 Performance Line family operates in the –40 to +105°C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows to design low-power applications.

The complete STM32F103 Performance Line family includes devices in 4 different package types: from 48 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103 Performance Line microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical and handheld equipment
- PC peripherals and medical monitors
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

Figure 1 shows the general block diagram of the device family.



2.1 Device summary

Table 1. Device features and peripheral counts (STM32F103 Performance Line)

Peripheral		STM32F103Cx		STM32F103Rx			STM32F103Vx	
Flash - Kbytes		32	64	32	64	128	64	128
SRAM - Kbytes		10	20	10	20		20	
Timers	General purpose	2	3	2	3		3	
	Advanced Control	1		1			1	
Communication	SPI	1	2	1	2		2	
	I ² C	1	2	1	2		2	
	USART	2	3	2	3		3	
	USB	1 ¹⁾	1	1 ¹⁾	1		1	
	CAN	1 ¹⁾	1	1 ¹⁾	1		1	
12-bit synchronized ADC		2		2			2	
CPU frequency		72 MHz						
Operating Voltage		2.0 to 3.6 V						
Operating Temp.		-40 to +85 °C / -40 to +105 °C						
Packages		LQFP48		LQFP64			LQFP100, BGA100	

1 For 32 KB Flash devices, CAN and USB are optional. The addition of coding “M” signifies the device selection without CAN and USB (for example STM32F10MC6x, and STM32F10MR6x). In these cases, the available SRAM is reduced to 6 Kbytes.

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2.2 Overview

ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F103 Performance Line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

Embedded Flash Memory

- Up to 128 Kbytes of embedded Flash is available in Bank 0 for storing programs and data.

Embedded SRAM

Up to 20 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

Nested Vectored Interrupt Controller (NVIC)

The STM32F103 Performance Line embeds a Nested Vectored Interrupt Controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

External Interrupts (EXTI)

The external interrupt controller consists of 19 edge detectors used to generate interrupt requests.

Each interrupt line can be independently configured to select the trigger event (rising or falling or both) and can be masked independently. A pending register maintains the status of the interrupt requests.

Up to 80 GPIOs are connected to the 16 external interrupt lines.

Clocks and start-up

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected and is monitored for failure. During such a scenario, it is disabled and software interrupt management follows. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the High Speed APB (APB2) and the low Speed APB (APB1) domains. The maximum frequency of the AHB and the High Speed APB domains is 72 MHz. The maximum allowed frequency of the Low Speed APB domain is 36 MHz.

Boot modes

At start-up, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from SystemMemory
- Boot from SRAM

Alternatively, the STM32F103 Performance Line can boot from the internal boot loader which triggers a boot from USART.

Power Supply Schemes

- VDD = 2.0 to 3.6 V: External Power Supply for I/Os and the internal regulator. Provided externally through VDD pins.
- VSSA, VDDA = 2.0 to 3.6 V: External Analog Power supplies for ADC, Reset blocks, RCs and PLL. In VDD range (ADC is limited at 2.4 V).
- VBAT= 2.0 to 3.6 V: Power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when VDD is not present.

Voltage Regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (RUN)
- LPR is used in the STOP modes.
- Power down is used in Standby Mode: the regulator output is in high impedance: the kernel circuitry is powered-down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after RESET. It is disabled in Standby Mode, providing high impedance output.

DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I²C, USART, general purpose and advanced control timers TIMx and ADC.

RTC (Real-Time Clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on VDD supply when present or through the VBAT pin. The backup registers (ten 16-bit registers) can be used to store data when VDD power is not present.

The Real-Time Clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by an external 32.768 kHz oscillator, the internal low power RC oscillator or the High Speed External clock divided by 128. The internal low power RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

Independent Watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in STOP and STANDBY modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application time out management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window Watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick Timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

General Purpose Timers (TIMx)

There are up to 3 synchronizable standard timers embedded in the STM32F103 Performance Line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one pulse mode output. This gives up to 12 input captures / output compares / PWMs on the largest packages. They can work together with the Advanced Control Timer via the Timer Link feature for synchronization or event chaining.

Any of the standard timers can be used to generate PWM outputs. Each of the timers has independent DMA request generations.

Advanced Control Timer (TIM1)

The Advanced Control Timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It can also be seen as a complete General Purpose timer. The 4 independent channels can be used for

- Input Capture
- Output Compare
- PWM generation (edge or center-aligned modes)
- One Pulse Mode output
- Complementary PWM Outputs with programmable inserted dead-times.

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

Many features are shared with those of the standard TIM timers which have the same architecture. The Advanced Control Timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

I²C bus

Up to two I²C bus interfaces can operate in multi-master and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

Universal Synchr./Asynch. Receiver Transmitter (USART)

One of the USART interfaces is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, IrDA SIR ENDEC support, are ISO 7816 compliant and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

Serial Peripheral Interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 8-bit to 16-bit. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

Controller Area Network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has two receive FIFOs with 3 stages and 14 scalable filter banks. Up to 32 message objects are handled through an internal SRAM buffer.

Universal Serial Bus (USB)

The STM32F103 Performance Line embeds a USB device peripheral compatible with the USB Full-speed 12 Mbs. The USB interface implements a full speed (12 Mbit/s) function

interface. It has software configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock source is generated from the internal main PLL.

GPIOs (General Purpose Input/Output)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as Peripheral Alternate Function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

I/Os on APB2 with up to 18 MHz toggling speed

Low Power modes

The STM32F103 Performance Line supports 4 low power modes.

- 2 **SLEEP** modes (CPU CLK is powered-off, Voltage regulator remains on)
- **STOP** (all clocks are stopped except IWDGCLK and RTCCLK)
- **STANDBY** (V_{18} domain and voltage regulator are powered-off)

ADC (Analog to Digital Converter)

Two 12-bit Analog to Digital Converters are embedded into STM32F103 Performance Line devices and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the standard timers (TIMx) and the Advanced Control timer (TIM1) can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

Temperature sensor

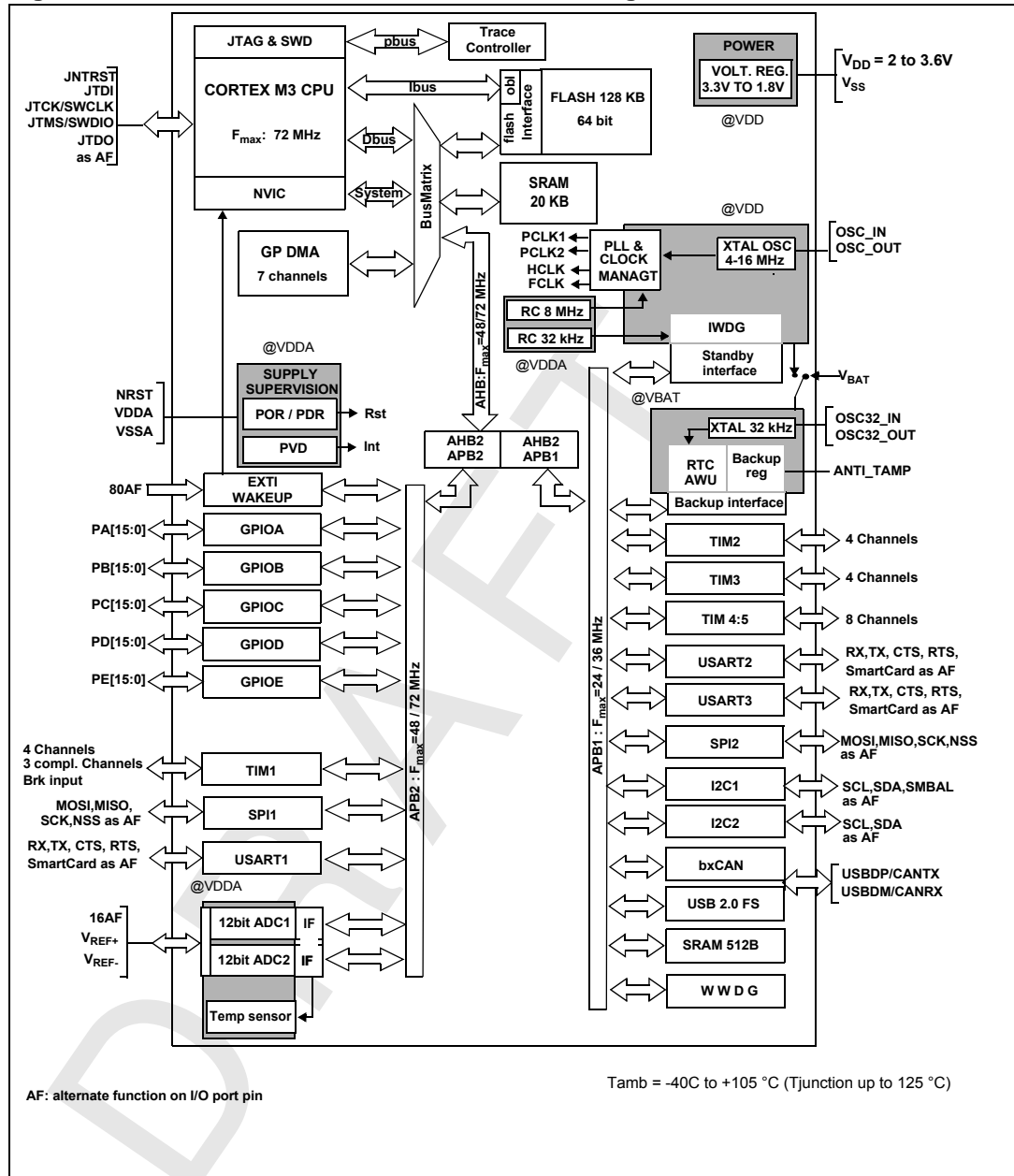
The temperature sensor has to generate a linear voltage with any variation in temperature. The conversion range is between $2V < V_{DDA} < 3.6V$. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

Serial WireJTAG Debug Port (SWJ-DP)

The ARM SWJ-DP Interface is embedded. and is a combined JTAG and Serial Wire Debug Port that enables either a Serial Wire Debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 1. STM32F103 Performance Line Block Diagram



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3 Pin Descriptions

Figure 2. STM32F103 Performance Line LQFP100 Pinout

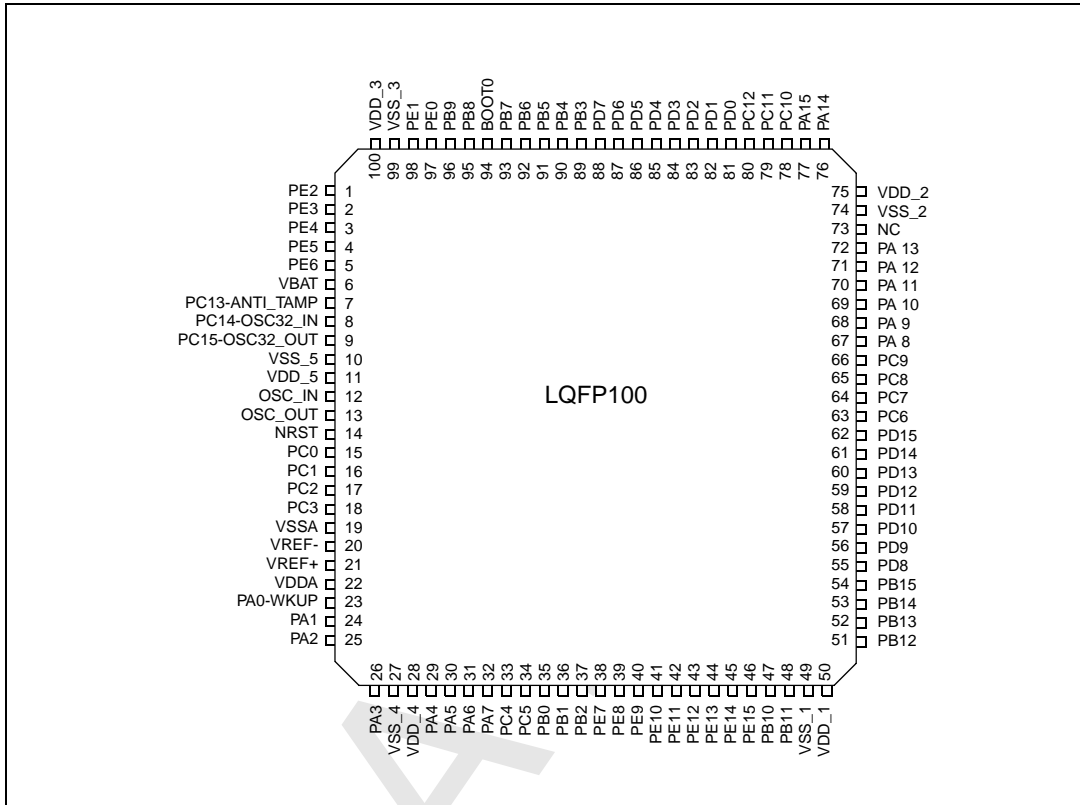
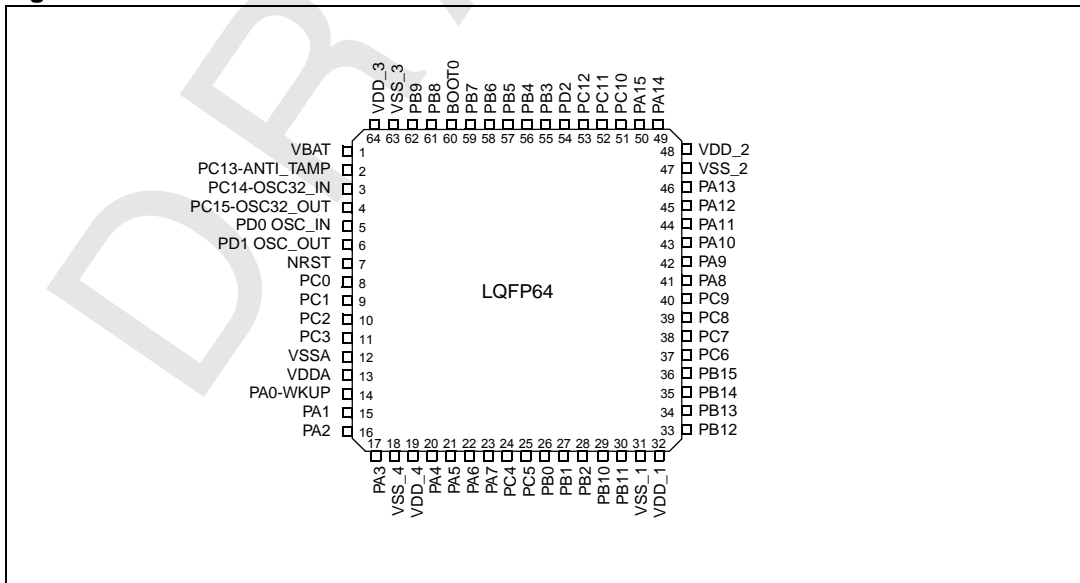


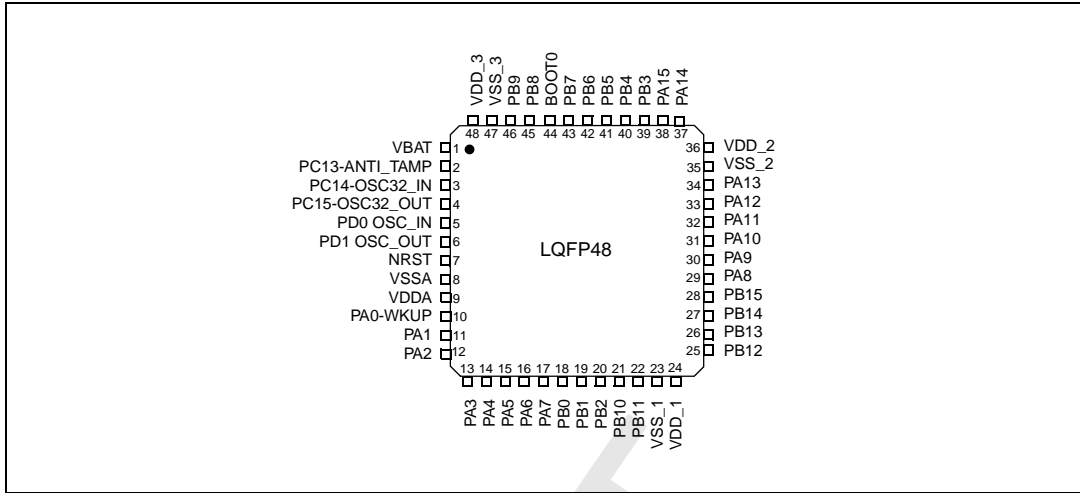
Figure 3. STM32F103 Performance Line LQFP64 Pinout



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Figure 4. STM32F103 Performance Line LQFP48 Pinout



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Legend / Abbreviations for Table 2:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: FT= 5 V tolerant

Note: Function availability depends on the chosen device. Refer to Table 1 on page 7.

Table 2. Pin Definitions

Pins			Pin Name	Type	I / O Level	Main function (after reset)	Default Alternate functions
LQFP48	LQFP64	LQFP100					
-	-	1	PE2/TRACECK	I/O	FT	PE2	TRACECK
-	-	2	PE3/TRACED0	I/O	FT	PE3	TRACED0
-	-	3	PE4/TRACED1	I/O	FT	PE4	TRACED1
-	-	4	PE5/TRACED2	I/O	FT	PE5	TRACED2
-	-	5	PE6/TRACED3	I/O	FT	PE6	TRACED3
1	1	6	VBAT	S		VBAT	
2	2	7	PC13-ANTI_TAMP	I/O		PC13	ANTI_TAMP
3	3	8	PC14-OSC32_IN	I/O		PC14-OSC32_IN	
4	4	9	PC15-OSC32_OUT	I/O		PC15-OSC32_OUT	
-	-	10	VSS_5	S		VSS_5	
-	-	11	VDD_5	S		VDD_5	
5	5	12	OSC_IN	I		OSC_IN	
6	6	13	OSC_OUT	O		OSC_OUT	
7	7	14	NRST	I/O		NRST	
-	8	15	PC0/ADC_IN10	I/O		PC0	ADC_IN10
-	9	16	PC1/ADC_IN11	I/O		PC1	ADC_IN11
-	10	17	PC2/ADC_IN12	I/O		PC2	ADC_IN12
-	11	18	PC3/ADC_IN13	I/O		PC3	ADC_IN13
8	12	19	VSSA	S		VSSA	
-	-	20	VREF-	S		VREF-	
-	-	21	VREF+	S		VREF+	
9	13	22	VDDA	S		VDDA	
10	14	23	PA0-WKUP/USART2_CTS/ ADC_IN0/TIM2_CH1_ETR	I/O		PA0	WKUP/USART2_CTS/ADC_IN0/ TIM2_CH1_ETR
11	15	24	PA1/USART2_RTS/ADC_IN1 /TIM2_CH2	I/O		PA1	USART2_RTS/ADC_IN1/TIM2_CH2
12	16	25	PA2/USART2_TX/ADC_IN2/ TIM2_CH3	I/O		PA2	USART2_TX/ADC_IN2/TIM2_CH3
13	17	26	PA3/USART2_RX/ADC_IN3/ TIM2_CH4	I/O		PA3	USART2_RX/ADC_IN3/TIM2_CH4
-	18	27	VSS_4	S		VSS_4	
-	19	28	VDD_4	S		VDD_4	

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Table 2. Pin Definitions (continued)

Pins			Pin Name	Type	I / O Level	Main function (after reset)	Default Alternate functions
LQFP48	LQFP64	LQFP100					
14	20	29	PA4/SPI1_NSS/ USART2_CK/ADC_IN4	I/O		PA4	SPI1_NSS/USART2_CK/ADC_IN4
15	21	30	PA5/SPI1_SCK/ADC_IN5	I/O		PA5	SPI1_SCK/ADC_IN5
16	22	31	PA6/SPI1_MISO/ADC_IN6/ TIM3_CH1	I/O		PA6	SPI1_MISO/ADC_IN6/TIM3_CH1
17	23	32	PA7/SPI1_MOSI/ADC_IN7/ TIM3_CH2	I/O		PA7	SPI1_MOSI/ADC_IN7/TIM3_CH2
-	24	33	PC4/ADC_IN14	I/O		PC4	ADC_IN14
-	25	34	PC5/ADC_IN15	I/O		PC5	ADC_IN15
18	26	35	PB0/ADC_IN8/TIM3_CH3	I/O		PB0	ADC_IN8/TIM3_CH3
19	27	36	PB1/ADC_IN9/TIM3_CH4	I/O		PB1	ADC_IN9/TIM3_CH4
20	28	37	PB2 / BOOT1	I/O	FT	PB2/BOOT1	
-	-	38	PE7	I/O	FT	PE7	
-	-	39	PE8	I/O	FT	PE8	
-	-	40	PE9	I/O	FT	PE9	
-	-	41	PE10	I/O	FT	PE10	
-	-	42	PE11	I/O	FT	PE11	
-	-	43	PE12	I/O	FT	PE12	
-	-	44	PE13	I/O	FT	PE13	
-	-	45	PE14	I/O	FT	PE14	
-	-	46	PE15	I/O	FT	PE15	
21	29	47	PB10/I2C2_SCL/ USART3_TX	I/O	FT	PB10	I2C2_SCL /USART3_TX
22	30	48	PB11/I2C2_SDA / USART3_RX	I/O	FT	PB11	I2C2_SDA/USART3_RX
23	31	49	VSS_1	S		VSS_1	
24	32	50	VDD_1	S		VDD_1	
25	33	51	PB12/SPI2_NSS / I2C2_SMBAL/ USART3_CK / TIM1_BKIN	I/O	FT	PB12	SPI2_NSS /I2C2_SMBAL/ USART3_CK /TIM1_BKIN
26	34	52	PB13/SPI2_SCK / USART3_CTS / TIM1_CH1N	I/O	FT	PB13	SPI2_SCK/USART3_CTS/ TIM1_CH1N
27	35	53	PB14/SPI2_MISO / USART3_RTS / TIM1_CH2N	I/O	FT	PB14	SPI2_MISO /USART3_RTS TIM1_CH2N
28	36	54	PB15/SPI2_MOSI TIM1_CH3N	I/O	FT	PB15	SPI2_MOSI/TIM1_CH3N
-	-	55	PD8	I/O	FT	PD8	
-	-	56	PD9	I/O	FT	PD9	
-	-	57	PD10	I/O	FT	PD10	
-	-	58	PD11	I/O	FT	PD11	

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Table 2. Pin Definitions (continued)

Pins			Pin Name	Type	I / O Level	Main function (after reset)	Default Alternate functions	
LQFP48	LQFP64	LQFP100						
-	-	59	PD12	I/O	FT	PD12		
-	-	60	PD13	I/O	FT	PD13		
-	-	61	PD14	I/O	FT	PD14		
-	-	62	PD15	I/O	FT	PD15		
-	37	63	PC6	I/O	FT	PC6		
	38	64	PC7	I/O	FT	PC7		
	39	65	PC8	I/O	FT	PC8		
-	40	66	PC9	I/O	FT	PC9		
29	41	67	PA8/USART1_CK/ TIM1_CH1/MCO	I/O	FT	PA8	USART1_CK/TIM1_CH1/MCO	
30	42	68	PA9/USART1_TX/ TIM1_CH2	I/O	FT	PA9	USART1_TX/TIM1_CH2	
31	43	69	PA10/USART1_RX/ TIM1_CH3	I/O	FT	PA10	USART1_RX/TIM1_CH3	
32	44	70	PA11 / USART1_CTS/ CANRX / USBDM ⁽¹⁾ / TIM1_CH4	I/O	FT	PA11	USART1_CTS/CANRX /TIM1_CH4 / USBDM ⁽¹⁾	
33	45	71	PA12 / USART1_RTS/ CANTX / USBDP ⁽¹⁾ / TIM1_ETR	I/O	FT	PA12	USART1_RTS/CANTX /TIM1_ETR / USBDP ⁽¹⁾	
34	46	72	PA13/JTMS/SWDIO	I/O	FT	JTMS/SWDIO	PA13	
-	-	73	Not connected					
35	47	74	VSS_2	S		VSS_2		
36	48	75	VDD_2	S		VDD_2		
37	49	76	PA14/JTCK/SWCLK	I/O	FT	JTCK/SWCLK	PA14	
38	50	77	PA15/JTDI	I/O	FT	JTDI	PA15	
-	51	78	PC10	I/O	FT	PC10		
-	52	79	PC11	I/O	FT	PC11		
-	53	80	PC12	I/O	FT	PC12		
5	5	81	PD0	I/O	FT	PD0		
6	6	82	PD1	I/O	FT	PD1		
	54	83	PD2/TIM3_ETR	I/O	FT	PD2	TIM3_ETR	
-	-	84	PD3	I/O	FT	PD3		
-	-	85	PD4	I/O	FT	PD4		
-	-	86	PD5	I/O	FT	PD5		
-	-	87	PD6	I/O	FT	PD6		
-	-	88	PD7	I/O	FT	PD7		
39	55	89	PB3/JTDO/TRACESWO	I/O	FT	JTDO	PB3/TRACESWO	
40	56	90	PB4/JNTRST	I/O	FT	JNTRST	PB4	
41	57	91	PB5/I2C1_SMBAL	I/O		PB5	I2C1_SMBAL	

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Table 2. Pin Definitions (continued)

Pins			Pin Name	Type	I/O Level	Main function (after reset)	Default Alternate functions
LQFP48	LQFP64	LQFP100					
42	58	92	PB6/I2C1_SCL/ TIM4_CH1	I/O	FT	PB6	I2C1_SCL/TIM4_CH1
43	59	93	PB7/I2C1_SDA/ TIM4_CH2	I/O	FT	PB7	I2C1_SDA/TIM4_CH2
44	60	94	BOOT0	I		BOOT0	
45	61	95	PB8/TIM4_CH3	I/O	FT	PB8	TIM4_CH3
46	62	96	PB9/TIM4_CH4	I/O	FT	PB9	TIM4_CH4
-	-	97	PE0/TIM4_ETR	I/O	FT	PE0	TIM4_ETR
-	-	98	PE1	I/O	FT	PE1	
47	63	99	VSS_3	S		VSS_3	
48	64	100	VDD_3	S		VDD_3	

Note: 1 CAN and USB alternate functions are not available on STM32F10MC6T6 and STM32F10MR6T6 devices.

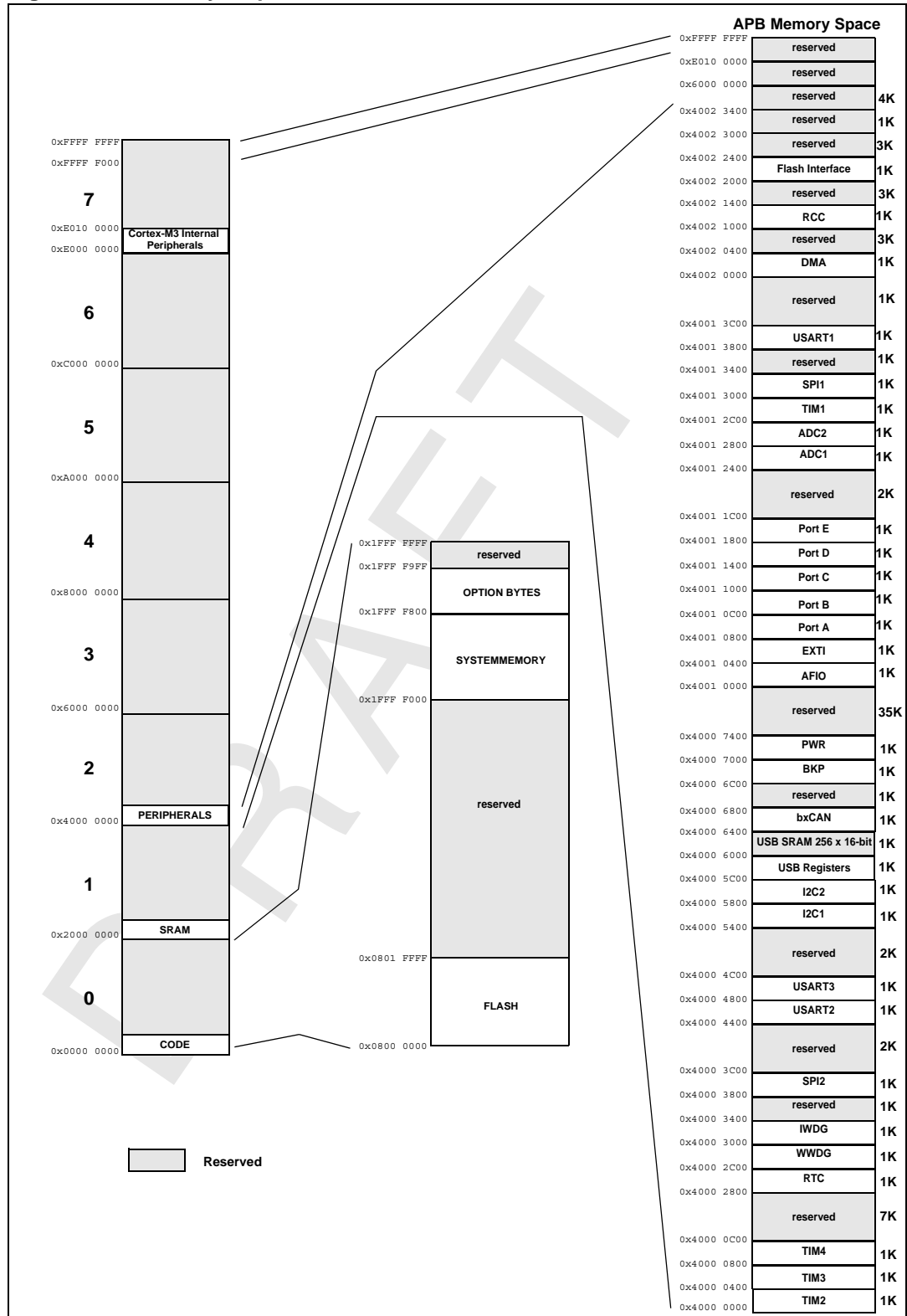
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4 Memory Mapping

Figure 5. Memory Map



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5 Electrical characteristics

5.1 Test conditions

Unless otherwise specified, all voltages are referred to V_{SS} .

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A=25^\circ\text{C}$ and $T_A=T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean}\pm 3\Sigma$).

5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A=25^\circ\text{C}$, $V_{DD}=3.3\text{ V}$ (for the $2\text{V}\leq V_{DD}\leq 3.6\text{V}$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean}\pm 2\Sigma$).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 6](#).

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 7](#).

Figure 6. Pin loading conditions

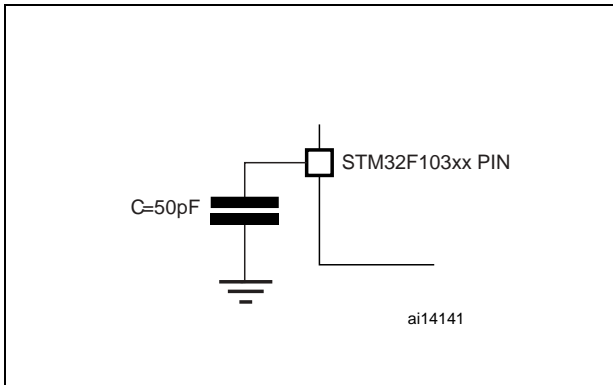
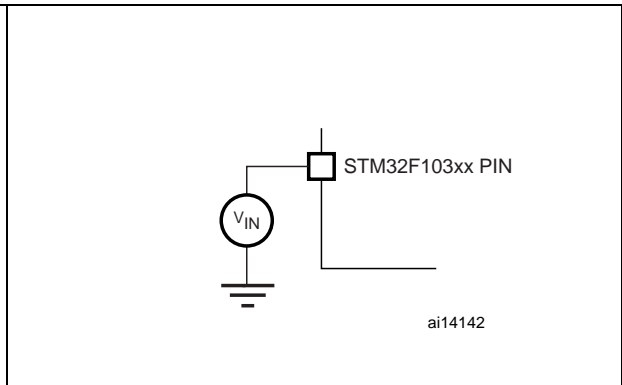
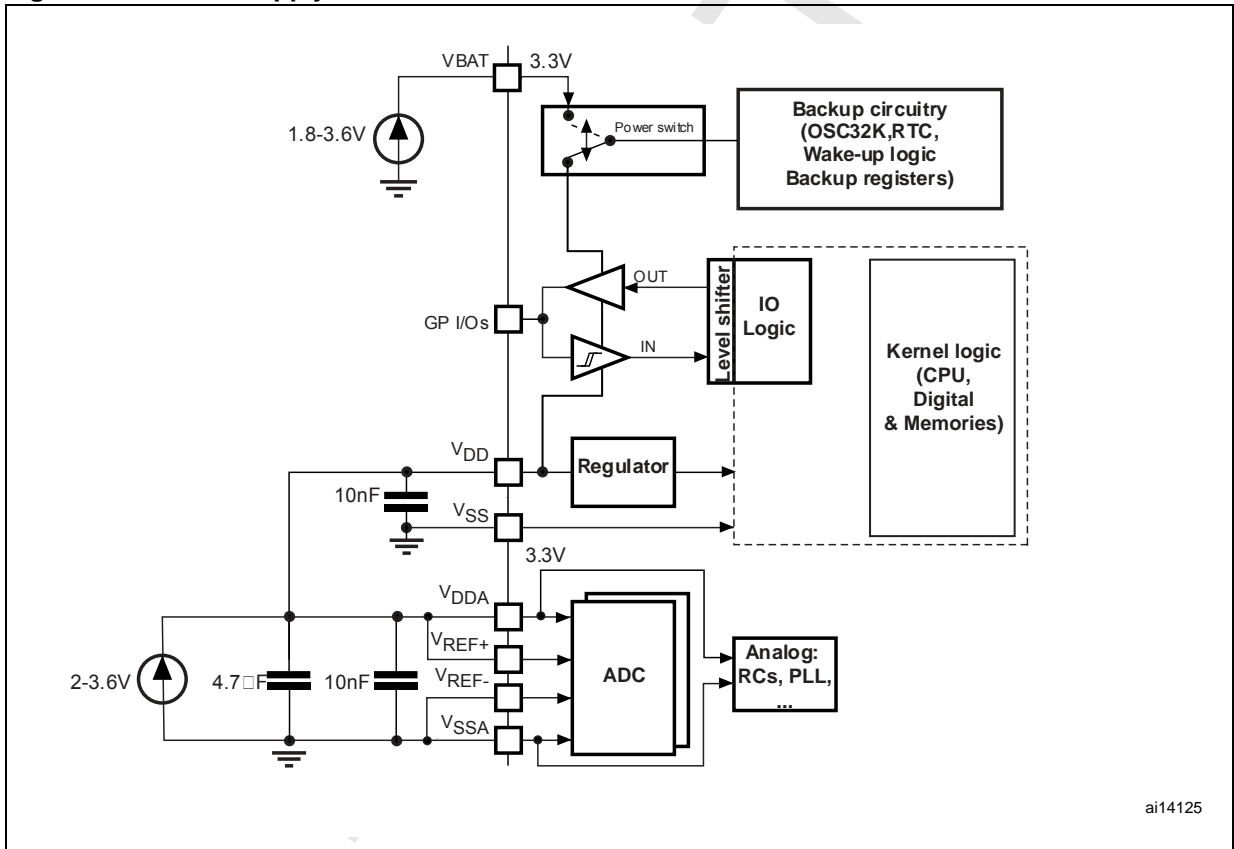


Figure 7. Pin input voltage



5.1.6 Power supply scheme

Figure 8. Power supply scheme

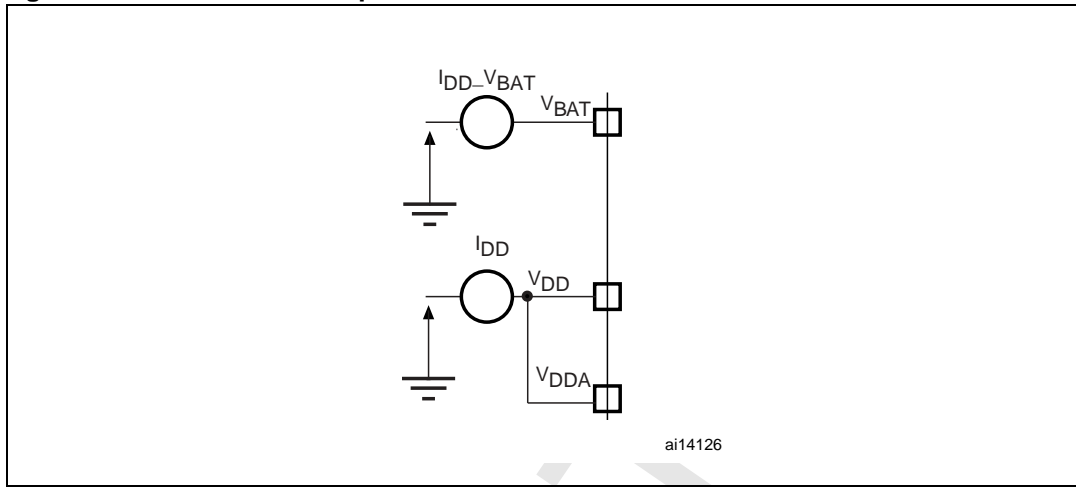


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5.1.7 Current consumption measurement

Figure 9. Current consumption measurement scheme



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5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 3: Voltage characteristics](#), [Table 4: Current characteristics](#), and [Table 5: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External 3.3V Supply voltage (including V_{DDA} and V_{DD}) ⁽¹⁾	-0.3	4.0	V
V_{IN}	Input voltage on five volt tolerant pin ⁽²⁾	$V_{SS} - 0.3$	+5.5	
	Input voltage on any other pin ⁽²⁾	$V_{SS} - 0.3$	$V_{DD}+0.3$	
$ \Delta V_{DDx} $	Variations between different power pins	50	50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins	50	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	see Section 5.3.11: Absolute Maximum Ratings (Electrical Sensitivity)		

- All 3.3V power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external 3.3V supply.
- $I_{INJ(PIN)}$ must never be exceeded (see [Table 4: Current characteristics](#)). This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

Table 4. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source) ⁽¹⁾	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) ⁽¹⁾	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$ ⁽²⁾⁽³⁾	Injected current on NRST pin	± 5	
	Injected current on HSE OSC_IN and LSE OSC_IN pins	± 5	
	Injected current on any other pin ⁽⁴⁾	± 5	
$\Sigma I_{INJ(PIN)}$ ⁽²⁾	Total injected current (sum of all I/O and control pins) ⁽⁴⁾	± 25	

- All 3.3V power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external 3.3V supply.
- $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
- Negative injection disturbs the analog performance of the device. See note in [Section 5.3.17: 12-bit ADC characteristics](#).
- When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 5. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (see Thermal characteristics)		

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5.3 Operating conditions

5.3.1 General operating conditions

Table 6. General operating conditions⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal system clock frequency		0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	36	
f_{PCLK2}	Internal APB2 clock frequency		0	72	
V_{DD}	Standard Operating Voltage		2	3.6	V
V_{BAT}	Backup Operating Voltage		1.8	3.6	V
T_A	Ambient temperature range		-40	105	°C

1. Data guaranteed by characterization, not tested in production

5.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 7](#) are derived from tests performed under the ambient temperature condition summarized in [Table 6](#).

Table 7. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate		20			μs/V
					20	ms/V

5.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 8](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 6](#).

Table 8. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable Voltage Detector Level Selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V		
$V_{PVDhyst}$	PVD hysteresis			100		mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$	PDR hysteresis			40		mV
$T_{RSTTEMPO}$	Reset temporization		1.5	2.5	3.5	mS

5.3.4 Embedded reference voltage

The parameters given in [Table 9](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 6](#).

Table 9. Embedded bandgap reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BG}	BandGap reference voltage	$-45^{\circ}\text{C} < T_A < +105^{\circ}\text{C}$	1.16	1.20	1.26	V
		$-45^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$	1.16	1.20	1.24	V

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5.3.5 Supply current characteristics

The current consumption is measured as described in [Figure 9: Current consumption measurement scheme](#).

Maximum Current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)

The parameters given in [Table 10](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 6](#).

Table 10. Maximum current consumption in RUN and SLEEP modes⁽¹⁾

Symbol	Parameter	Conditions	F _{HCLK}	Typ ⁽²⁾	Max ⁽³⁾		Unit
					TA 85°C	TA 105°C	
I _{DD}	Supply current in RUN mode	External clock with PLL, code running from Flash, all peripheral enabled (see RCC register description): $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$	72 MHz	36	TBD	TBD	mA
			48 MHz	30	TBD	TBD	
			36 MHz	TBD	TBD	TBD	
			24 MHz	21	TBD	TBD	
			8 MHz	10	TBD	TBD	
	Supply current in SLEEP mode	External clock with PLL, code running from RAM or Flash, all peripheral enabled (see RCC register description): $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$	72 MHz	32	TBD	TBD	
			48 MHz	22	TBD	TBD	
			36 MHz	TBD	TBD	TBD	
			24 MHz	11	TBD	TBD	
			8 MHz	4.5	TBD	TBD	
Supply current in SLEEP mode	External clock with PLL, code running from RAM or Flash, all peripheral enabled (see RCC register description): $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$	72 MHz	22	TBD	TBD	mA	
		48 MHz	TBD	TBD	TBD		
		36 MHz	TBD	TBD	TBD		
		24 MHz	TBD	TBD	TBD		
		8 MHz	3.5	TBD	TBD		

1. TBD stands for To Be Defined.
2. Typical values are measured at $T_A = 25^\circ\text{C}$, and $V_{DD} = 3.3\text{V}$
3. Data based on characterization results, tested in production at V_{DDmax} , $f_{HCLKmax}$ and T_Amax .

Figure 10. RUN mode current consumption versus frequency (PLL off from 4 to 16 MHz at 3.3 V and 25 °C, 85 °C and 105 °C)

Figure 11. RUN mode current consumption versus frequency (from 16 to 72 MHz at 3.3 V and 25 °C, 85 °C and 105 °C)

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Table 11. Maximum current consumption in STOP and STANDBY modes⁽¹⁾

Symbol	Parameter	Conditions	Typ ⁽²⁾		Max ⁽³⁾		Unit
			V _{DD} / V _{BAT} = 2.4V	V _{DD} / V _{BAT} = 3.3V	T _A = 85°C	T _A = 105°C	
I _{DD}	Supply current in STOP mode	Regulator in RUN mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independant watchdog)	TBD	24	TBD	TBD	μA
		Regulator in Low Power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independant watchdog)	TBD	14	TBD	TBD	
	Supply current in STANDBY mode ⁽⁴⁾	Low-speed internal RC oscillator and independant watchdog OFF, low-speed oscillator and RTC OFF	TBD	2	TBD	TBD	
I _{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1	1.4	TBD	TBD	

1. TBD stands for To Be Defined.
2. Typical values are measured at T_A=25 °C, V_{DD}=3.3 V, unless otherwise specified.
3. Data based on characterization results, tested in production at V_{DD} max, f_{HCLK} max. and T_A max (for other temperature refer to Figure 12 and Figure 13).
4. To have the STANDBY consumption with RTC ON, add I_{DD_VBAT} (Low-speed oscillator and RTC ON) to I_{DD} STANBY (when V_{DD} is present the Backup Domain is powered by V_{DD} supply).

Figure 12. Current consumption in STOP mode with regulator in Run Mode (at V_{DD} = 3.3 V, 2.4 V and 2.0 V) versus temperature (-40 to 105 °C)

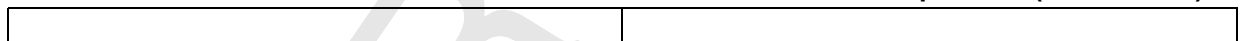
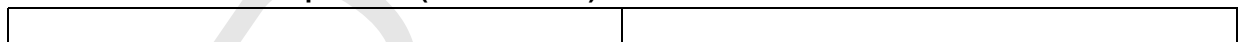


Figure 13. Current consumption in STOP mode with regulator in Low Power mode (at V_{DD} = 3.3 V, 2.4 V and 2.0 V) versus temperature (-40 to 105°C)

Figure 14. Current consumption in STANDBY mode (at V_{DD} = 3.3 V, 2.4 V and 2.0 V) versus temperature (-40 to 105 °C)

Figure 15. VBAT Backup domain consumption (at V_{BAT} = 3.3 V, 2.4 V and 1.8 V) versus temperature (-40 to 105 °C)



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Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).
- Ambient temperature and V_{DD} supply voltage conditions summarized in [Table 6](#).

Table 12. Typical current consumption in RUN and SLEEP modes⁽¹⁾

Symbol	Parameter	Conditions	f_{HCLK}	Typ ⁽²⁾	Unit
I_{DD}	Supply current in RUN mode	Oscillator running at 8 MHz with PLL, code running from Flash, all peripheral disabled (see RCC register description): $f_{PCLK1}=f_{HCLK}/2$, $f_{PCLK2}=f_{HCLK}$	72 MHz ⁽³⁾	21	mA
			48 MHz ⁽³⁾	18	
			36 MHz	TBD	
			24 MHz	13	
			16 MHz	TBD	
		Running on HSI clock, code running from Flash, all peripheral disabled (see RCC register description): $f_{PCLK1}=f_{HCLK}/2$, $f_{PCLK2}=f_{HCLK}$. AHB pre-scaler used to reduce the frequency	8 MHz	7.8	mA
			4 MHz	7	
			2 MHz	6.3	
			1 MHz	6.2	
			500 kHz	6.1	
	Running on HSI clock, code running from RAM, all peripheral disabled (see RCC register description): $f_{PCLK1}=f_{HCLK}/2$, $f_{PCLK2}=f_{HCLK}$. AHB pre-scaler used to reduce the frequency	8 MHz	2.3	mA	
		4 MHz	1.6		
		2 MHz	1.2		
		1 MHz	1		
		500 kHz	0.88		
	Supply current in SLEEP mode	Oscillator running at 8MHz with PLL, code running from Flash, all peripheral disabled (see RCC register description): $f_{PCLK1}=f_{HCLK}/2$, $f_{PCLK2}=f_{HCLK}$	72 MHz ⁽³⁾	6	mA
			48 MHz ⁽³⁾	TBD	
			36 MHz	TBD	
			24 MHz	TBD	
			16 MHz	1	
Running on HSI clock, code running from Flash, all peripheral disabled (see RCC register description): $f_{PCLK1}=f_{HCLK}/2$, $f_{PCLK2}=f_{HCLK}$. AHB pre-scaler used to reduce the frequency		8 MHz	TBD	mA	
		4 MHz	TBD		
		2 MHz	TBD		
		1 MHz	TBD		
		500 kHz	TBD		

1. TBD stands for To Be Defined.

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- 2. Typical values are measures at $T_A=25\text{ }^\circ\text{C}$, $V_{DD}=3.3\text{ V}$.
- 3. Data based on characterization results, tested in production at V_{DD} , f_{HCLK} max. and T_A max.

Table 13. Typical current consumption in STOP and STANDBY modes⁽¹⁾

Symbol	Parameter	Conditions	V_{DD}	Typ ⁽²⁾
I_{DD}	Supply current in STOP mode	Regulator in RUN mode, Low-speed and high-speed internal RC oscillators OFF High-speed oscillator OFF (no independant watchdog)	3.3 V	24
			2.4 V	TBD
		Regulator in Low Power mode, Low-speed and high-speed internal RC oscillators OFF, High-speed oscillator OFF (no independant watchdog)	3.3 V	14
			2.4 V	TBD
	Supply current in STANDBY mode ⁽³⁾	Low-speed internal RC oscillator and independant watchdog OFF	3.3 V	2
			2.4 V	TBD
		Low-speed internal RC oscillator and independant watchdog ON	3.3 V	3.1
			2.4 V	TBD
		Low-speed internal RC oscillator ON, independant watchdog OFF	3.3 V	2.9
			2.4 V	TBD
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	3.3 V	1.4
			2.4 V	1
		Low-speed oscillator OFF, RTC ON	3.3 V	0.5
			2.4 V	TBD

- 1. TBD stands for To Be Defined.
- 2. Typical values are measures at $T_A=25\text{ }^\circ\text{C}$, $V_{DD}=3.3\text{ V}$.
- 3. To obtain STANDBY consumption with RTC ON, add I_{DD_VBAT} (Low-speed oscillator and RTC ON) to I_{DD} STANBY.

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On-Chip Peripherals current consumption

The current consumption of the on-chip peripherals are given in [Table 14](#). They are derived from tests performed under following conditions:

- $V_{DD} = V_{DDA} = 3.3\text{ V}$
- $T_A = 25\text{ °C}$

Table 14. Peripheral current consumption⁽¹⁾

Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 Timer supply current ⁽²⁾	TBD	mA / MHz
$I_{DD(TIM2)}$	TIM2 Timer supply current ⁽³⁾	TBD	
$I_{DD(USART1)}$	USART1 supply current ⁽⁴⁾	TBD	
$I_{DD(USART2)}$	USART2 supply current ⁽⁵⁾	TBD	
$I_{DD(SPI1)}$	SPI1 supply current ⁽⁶⁾	TBD	
$I_{DD(SPI2)}$	SPI2 supply current ⁽⁷⁾	TBD	
$I_{DD(I2C1)}$	I2C1 supply current ⁽⁸⁾	TBD	
$I_{DD(ADC1)}$	ADC1 supply current when converting ⁽⁹⁾	TBD	
$I_{DD(USB)}$	USB supply current ⁽¹⁰⁾ Note: V_{DD} must be $\pm 10\%$	TBD	
$I_{DD(BxCAN)}$	BxCAN supply current when converting ⁽¹¹⁾	TBD	
$I_{DD(TS)}$	Temperature Sensor current ⁽¹²⁾	TBD	

1. TBD stands for To Be Defined.
2. Value based on a differential I_{DD} measurement between reset configuration and timer counter running at 72 MHz. No IC/OC programmed (no I/O pads toggling).
3. Value based on a differential I_{DD} measurement between reset configuration and timer counter running at 36 MHz. No IC/OC programmed (no I/O pads toggling). TIM3 and TIM4 supply currents are identical to $I_{DD(TIM2)}$.
4. Value based on a differential I_{DD} measurement between the reset configuration and permanent USART1 data transmit sequence at 4.5 Mbauds. This measurement does not include the pad toggling consumption.
5. Value based on a differential I_{DD} measurement between the reset configuration and permanent USART2 data transmit sequence at 2.25 Mbauds. This measurement does not include the pad toggling consumption. USART3 supply current is identical to $I_{DD(USART2)}$.
6. Value based on a differential I_{DD} measurement between reset configuration and permanent SPI1 master communication at maximum speed 36 MHz. The data sent is 55h. This measurement does not include the pad toggling consumption.
7. Value based on a differential I_{DD} measurement between reset configuration and permanent SPI1 master communication at maximum speed 18 MHz. The data sent is 55h. This measurement does not include the pad toggling consumption.
8. Value based on a differential I_{DD} measurement between reset configuration and a permanent I2C master communication at 100 kHz (data sent equal to 55h). This measurement include the pad toggling consumption but not the external 10 k Ω external pull-up on clock data line.
9. Value based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions at 12 MHz in scan mode on 16 inputs configured as AIN.
10. Value based on a differential I_{DD} measurement between reset configuration and a running generic HID application.
11. Value based on a differential I_{DD} measurement between reset configuration and a permanent CAN data transmit sequence in loop back mode at 1 MHz. This measurement does not include the pad toggling consumption.
12. Data based on a differential I_{DD} measurement between reset configuration and Temperature Sensor enabled.

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5.3.6 External clock source characteristics

High-speed external user clock

The characteristics given in [Table 15](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 6](#).

Table 15. High-speed external (HSE) user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency ⁽¹⁾			8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time ⁽¹⁾		16			ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time ⁽¹⁾				5	
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			± 1	μA

1. Value based on design simulation and/or technology characteristics. It is not tested in production.

Low-speed external user clock

The characteristics given in [Table 16](#) result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 6](#).

Table 16. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency ⁽¹⁾			32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time ⁽¹⁾		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time ⁽¹⁾				5	
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			± 1	μA

1. Value based on design simulation and/or technology characteristics. It is not tested in production.

Figure 16. High-speed external clock source AC timing diagram

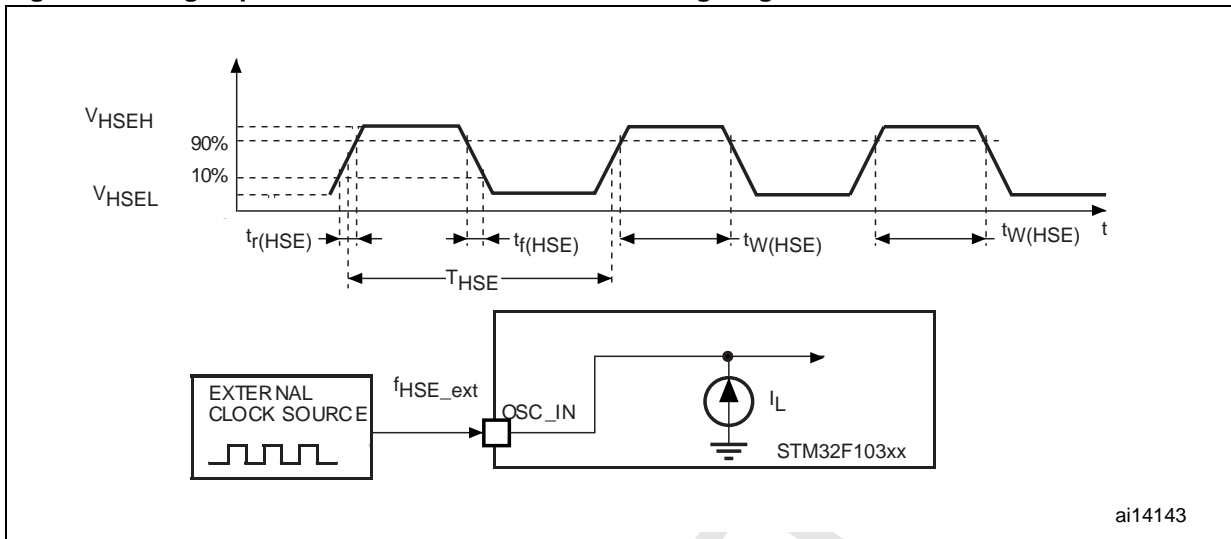
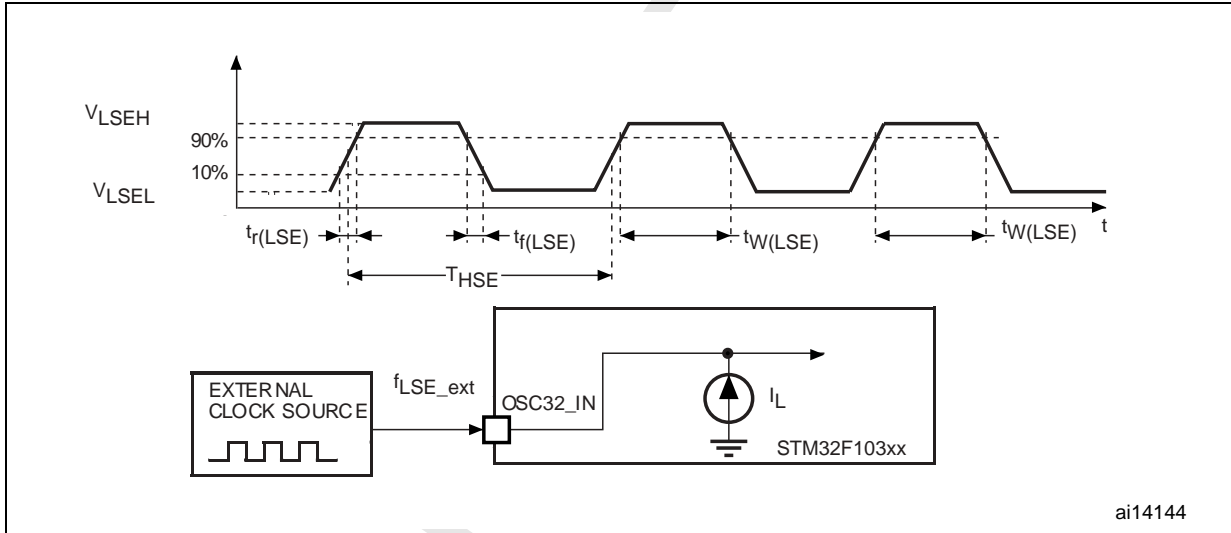


Figure 17. Low-speed external clock source AC timing diagram



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High-speed external clock

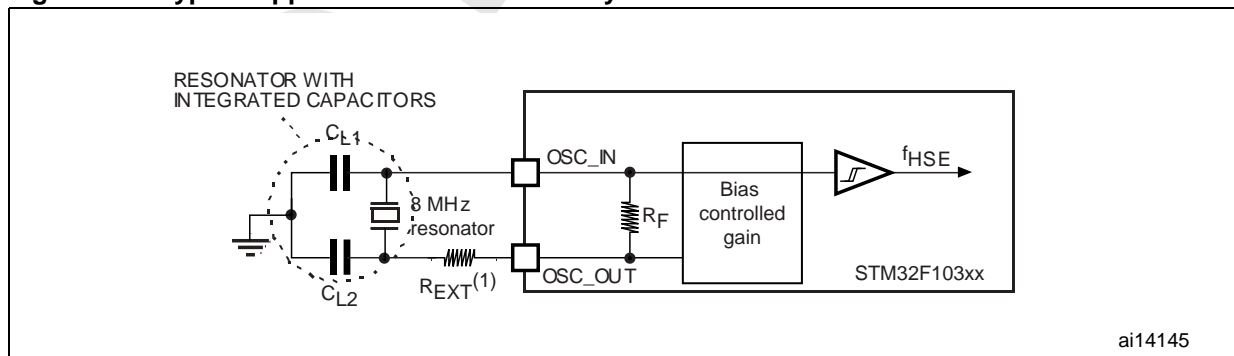
The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 17](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 17. HSE 4-16 MHz oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	16	MHz
R_F	Feedback resistor			200		k Ω
C_{L1} $C_{L2}^{(2)}$	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S) ⁽³⁾	$R_S=30\ \Omega$		30		pF
i_2	HSE driving current	$V_{DD}=3.3\ V$ $V_{IN}=V_{SS}$ with 30 pF load			1	mA
g_m	Oscillator Transconductance	Startup	25			mA/V
$t_{SU(LSE)}^{(4)}$	startup time	V_{SS} is stabilized		2		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 25pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included when sizing C_{L1} and C_{L2} (10 pF can be used as a rough estimate of the combined pin and board capacitance).
3. The relatively low value of the R_F resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(LSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 18. Typical application with a 8-MHz Crystal



1. R_{EXT} value depends on the crystal characteristics. Typical value is in the range of 5 to 6 R_S .

Low-speed external clock

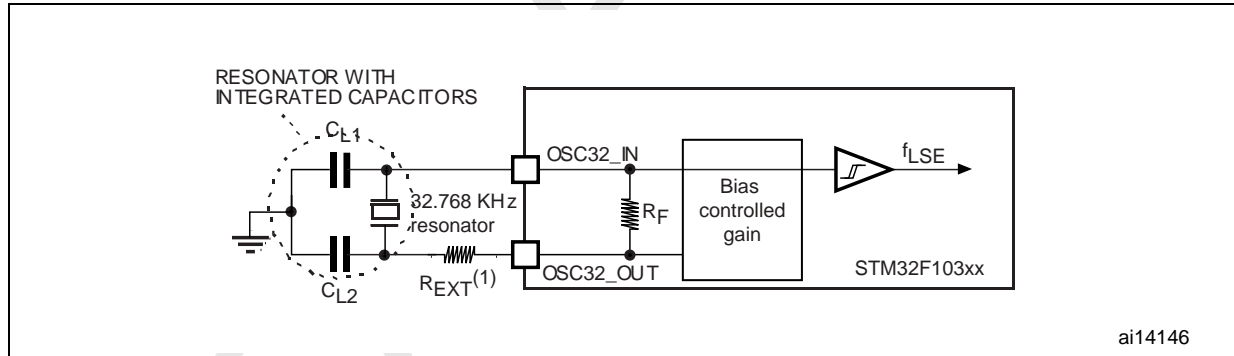
The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 18](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 18. LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor			5		$M\Omega$
C_{L1} C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S) ⁽¹⁾	$R_S = 30\text{ K}\Omega$			15	pF
I_2	LSE driving current	$V_{DD} = 3.3\text{ V}$ $V_{IN} = V_{SS}$			1.4	μA
g_m	Oscillator Transconductance		5			$\mu\text{A/V}$
$t_{SU(LSE)}$ ⁽²⁾	startup time	V_{SS} is stabilized		3		s

1. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
2. $t_{SU(LSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 19. Typical application with a 32.768 kHz crystal



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5.3.7 Internal Clock source characteristics

The parameters given in [Table 19](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 6](#).

High-speed internal (HSI) RC oscillator

Table 19. HSI oscillator characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max ⁽³⁾	Unit
f_{HSI}	Frequency			8		MHz
ACC_{HSI}	Accuracy of HSI oscillator	$T_A = -40$ to 105°C	-3		+3	%
		at $T_A = 25^\circ\text{C}$	-1		+1	%
$t_{su(HSI)}$	HSI oscillator start up time		1		2	μs
$I_{DD(HSI)}$	HSI oscillator power consumption			80	TBD	μA

- $V_{DD} = 3.3\text{ V}$, $T_A = -40$ to 105°C unless otherwise specified.
- TBD stands for To Be Defined.
- Values based on device characterization, not tested in production.

LSI Low Speed Internal RC Oscillator

Table 20. LSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max ⁽²⁾	Unit
f_{LSI}	Frequency		32		80	kHz
ACC_{LSI}	Accuracy of LSI oscillator					%
$t_{su(LSI)}$	LSI oscillator start up time				85	μs
$I_{DD(LSI)}$	LSI oscillator power consumption			0.65	1.2	μA

- $V_{DD} = 3\text{ V}$, $T_A = -40$ to 105°C unless otherwise specified.
- Value based on device characterization, not tested in production.

Wake-up time from low power mode

The wake-up times given in [Table 21](#) is measured on a wake-up phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 6](#).

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Table 21. Low-power mode wake-up timings⁽¹⁾

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}^{(2)}$	Wake-up from Sleep mode	Wake-up on HSI RC clock	0.75	TBD	μs
$t_{WUSTOP}^{(2)}$	Wake-up from Stop mode (regulator in run mode)	HSI RC wake-up time=2 μs	4	TBD	μs
	Wake-up from Stop mode (regulator in low power mode)	HSI RC wake-up time=2 μs , Regulator wake-up from LP mode time=5 μs	7	TBD	
$t_{WUSTDBY}^{(3)}$	Wake-up from Standby mode	HSI RC wake-up time=2 μs , Regulator wake-up from power down time=38 μs	40	TBD	μs

1. TBD stands for To Be Defined.
2. The wake-up time from Sleep and Stop mode are measured from the wake-up event to the point in which the user application code reads the first instruction.
3. The wake-up time from Standby mode is measured from the wake-up event to the point in which the device exits from reset.

5.3.8 PLL characteristics

The parameters given in [Table 22](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 6](#).

Table 22. PLL characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max ⁽¹⁾	
f_{PLL_IN}	PLL input clock			8.0		MHz
	PLL input clock duty cycle		40		60	%
f_{PLL_OUT}	PLL multiplier output clock		16		72	MHz
f_{VCO}	VCO frequency range	When PLL operates (locked)	32		144	MHz
t_{LOCK}	PLL lock time				200	μs
t_{JITTER}	Cycle to cycle jitter (+/-3 Σ peak to peak)	V_{DD} is stable	-3		+3	%

1. Data based on device characterization, not tested in production.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at $T_A = -40$ to 105 °C unless otherwise specified.

Table 23. Flash memory characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max ⁽²⁾	Unit
t_{prog}	Word programming time	$T_A = -40$ to $+105$ °C	20		40	µs
t_{ERASE}	Page (1kB) erase time	$T_A = -40$ to $+105$ °C	20		40	ms
t_{ME}	Mass erase time	$T_A = -40$ to $+105$ °C	20		40	ms
I_{DD}	Supply current	Read mode $f_{HCLK} = 72$ MHz with 2 wait states, $V_{DD} = 3.3$ V		TBD	20	mA
		Write / Erase modes $f_{HCLK} = 72$ MHz, $V_{DD} = 3.3$ V		TBD	5	mA
		Power-down mode / HALT, $V_{DD} = 3.0$ to 3.6 V		TBD	50	µA

1. TBD stands for To Be Defined.
2. Values based on characterization and not tested in production.

Table 24. Flash endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min ⁽¹⁾	Typ	Max	
N_{END}	Endurance		1			kcycles
t_{RET}	Data Retention	$T_A = 25$ ° C	100			Years

1. Values based on characterization not tested in production.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic Discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 1000-4-2 standard.
- **FTB: A Burst of Fast Transient voltage** (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 25](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 25. EMS characteristics⁽¹⁾

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD}=3.3\text{ V}$, $T_A=+25\text{ °C}$, $f_{HCLK}=48\text{ MHz}$ conforms to IEC 1000-4-2	TBD
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD}=3.3\text{ V}$, $T_A=+25\text{ °C}$, $f_{HCLK}=48\text{ MHz}$ conforms to IEC 1000-4-4	

1. TBD stands for To Be Defined.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with SAE J 1752/3 standard which specifies the test board and the pin loading.

Table 26. EMI data⁽¹⁾

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f _{HSE} /f _{HCLK}]		Unit
				8/48 MHz	8/72 MHz	
S _{EMI}	Peak level	V _{DD} =3.3 V, T _A =25 °C, LQFP100 package compliant with SAE J 1752/3	0.1MHz to 30 MHz	TBD		dB μ V
			30 MHz to 130 MHz			
			130 MHz to 1GHz			
			SAE EMI Level			-

1. TBD stands for To Be Defined.

5.3.11 Absolute Maximum Ratings (Electrical Sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic Discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n+1) supply pins). Two models can be simulated:

- Human Body Model
- Machine Model.

The tests are compliant with JESD22-A114A/A115A standard.

Table 27. ESD absolute maximum ratings⁽¹⁾

Symbol	Ratings	Conditions	Maximum value ⁽²⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (Human Body Model)	T _A =+25 °C	TBD	V
V _{ESD(CDM)}	Electrostatic discharge voltage (Charge Device Model)		TBD on corner pins, TBD on others	

1. TBD stands for To Be Defined.

2. Values based on characterization results, not tested in production.

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Static and Dynamic Latch-Up

- **Static latch-up (LU)**

Two complementary static tests are required on 10 parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

- **Dynamic latch-up (DLU)**

Electrostatic discharges (one positive then one negative test) are applied to each pin of 3 samples while the micro is running. Their objective is to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the MCU and the component is put in reset mode.

This test is compliant with IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Table 28. Electrical sensitivities⁽¹⁾

Symbol	Parameter	Conditions	Class ⁽²⁾
LU	Static latch-up class	T _A =+25°C T _A =+85°C T _A =+105°C	TBD TBD TBD
DLU	Dynamic latch-up class	V _{DD} =3.3V, f _{HSE} =8MHz, f _{HCLK} =48 MHz, T _A =+25°C	TBD

1. TBD stands for To Be Defined.
2. Class description: a class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

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5.3.12 I/O port pin characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 29](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 6](#).

All unused pins must be held at a fixed voltage, by using the I/O output mode, an external pull-up or pull-down resistor (see [Figure 22](#)).

Table 29. I/O static characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage ⁽²⁾	TTL ports	-0.5		0.8	V
V_{IH}	IO TC input high level voltage ⁽²⁾		2		$V_{DD}+0.5$	
	IO FT high level voltage ⁽²⁾		2		5.5V	
V_{IL}	Input low level voltage ⁽²⁾	CMOS ports	-0.5		$0.35 V_{DD}$	V
V_{IH}	Input high level voltage ⁽²⁾		$0.65 V_{DD}$		$V_{DD}+0.5$	
V_{hys}	IO TC Schmitt trigger voltage hysteresis ⁽³⁾			200		mV
	IO TC Schmitt trigger voltage hysteresis ⁽³⁾			$5\% V_{DD}$ ⁽⁴⁾		mV
I_{lkg}	Input leakage current ⁽⁴⁾	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os			± 1	μA
		$V_{IN} = 5V$ 5V tolerant I/Os			3	
R_{PU}	Weak pull-up equivalent resistor ⁽⁵⁾	$V_{IN} = V_{SS}$		40		$k\Omega$
R_{PD}	Weak pull-down equivalent resistor ⁽⁶⁾	$V_{IN} = V_{DD}$		40		$k\Omega$
C_{IO}	I/O pin capacitance			5		pF

- $V_{DD} = 3.3V$, $T_A = -40$ to 105 °C unless otherwise specified.
- Values based on characterization results, and not tested in production.
- Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
- With a minimum of 100 mV.
- Leakage could be higher than max. if negative current is injected on adjacent pins.
- Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10%order).

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Figure 20. R_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$

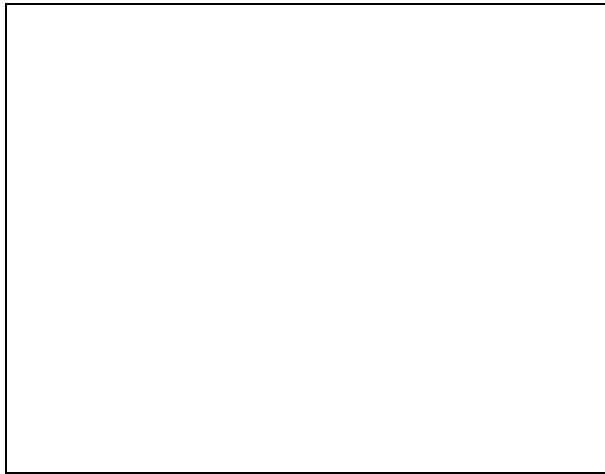
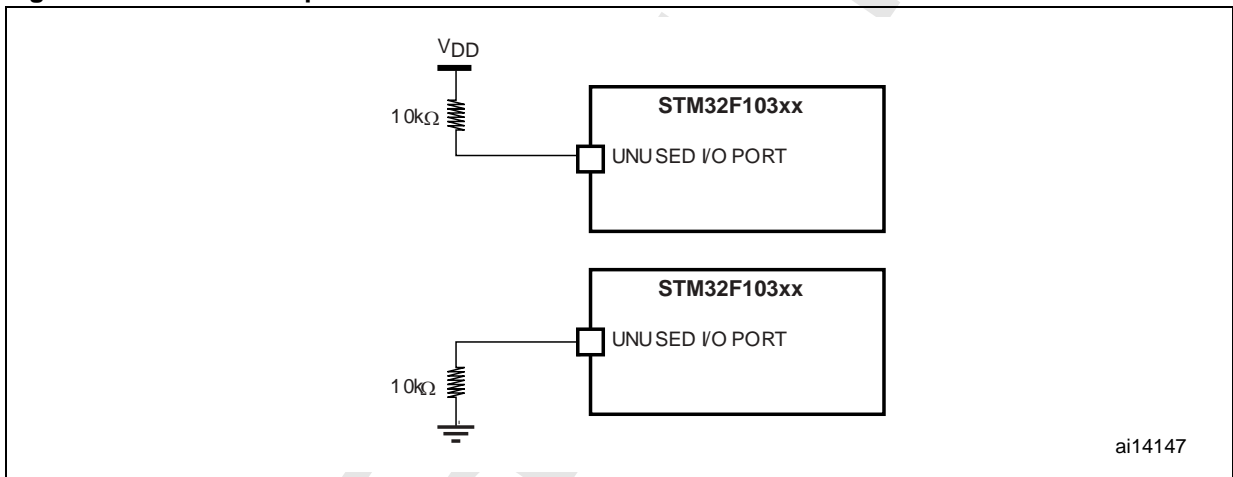


Figure 21. R_{PD} vs. V_{DD} with $V_{IN}=V_{DD}$



Figure 22. Unused I/O pin connection



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Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink +20 mA (with a relaxed V_{OL}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#):

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum RUN consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating I_{VDD} (see [Table 4](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum RUN consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see [Table 4](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 30](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 6](#).

Table 30. Output voltage characteristics ($2.7\text{ V} < V_{DD} < 3.6\text{ V}$)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time (see Figure 23)	TTL port $I_{IO}=+8\text{mA}$		0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 4 pins are sourced at same time (see Figure 23 and Figure 25)		$V_{DD}-0.4$		
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time (see Figure 23)	CMOS port $I_{IO}=+8\text{mA}$		0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 4 pins are sourced at same time (see Figure 23 and Figure 25)		2.4		
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time (see Figure 23)	$I_{IO}=+20\text{mA}$		1.3	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 4 pins are sourced at same time (see Figure 23 and Figure 25)		$V_{DD}-1.3$		

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 4](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 4](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .

Figure 23. Typical V_{OL} and V_{OH} at $V_{DD}=3.3\text{V}$



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Figure 24. Typical V_{OL} vs. V_{DD}



Figure 25. Typical V_{OH} vs. V_{DD}



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Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 26](#) and [Table 31](#), respectively.

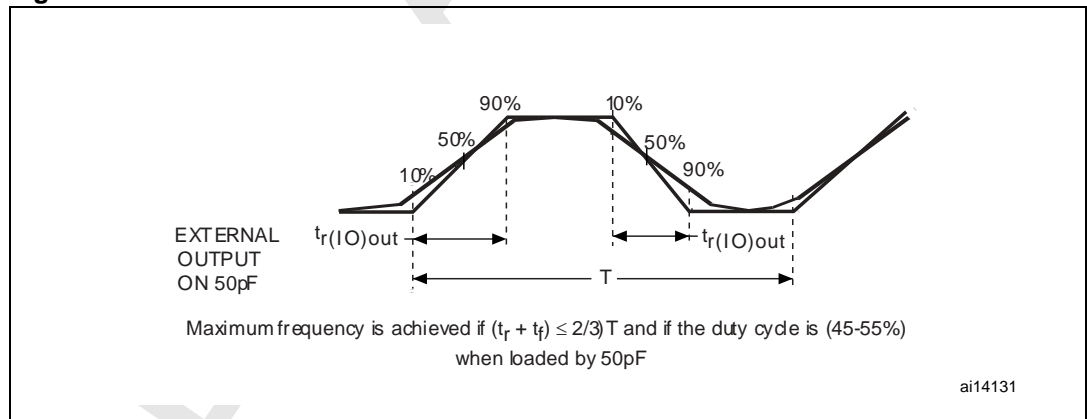
Unless otherwise specified, the parameters given in [Table 31](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 6](#).

Table 31. I/O AC characteristics for $V_{DD}= 2.7$ to $3.6V$

I/O Mode ⁽¹⁾	Symbol	Parameter	Conditions	Max	Unit
10	$f_{max(I/O)out}$	Maximum Frequency ⁽²⁾	$C_L=50$ pF	2	MHz
	$t_{f(I/O)out}$	Output high to low level fall time ⁽³⁾	$C_L=50$ pF Between 10% and 90%	125	ns
	$t_{r(I/O)out}$	Output low to high level rise time ⁽³⁾		125	
01	$f_{max(I/O)out}$	Maximum Frequency ⁽²⁾	$C_L=50$ pF	10	MHz
	$t_{f(I/O)out}$	Output high to low level fall time ⁽³⁾	$C_L=50$ pF Between 10% and 90%	25	ns
	$t_{r(I/O)out}$	Output low to high level rise time ^v		25	
11	$f_{max(I/O)out}$	Maximum Frequency ⁽²⁾	$C_L=30$ pF	50	MHz
	$t_{f(I/O)out}$	Output high to low level fall time ⁽³⁾	$C_L=30$ pF Between 10% and 90%	5	ns
	$t_{r(I/O)out}$	Output low to high level rise time ⁽³⁾		5	

1. Refer to the Reference user manual UM0427 for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 26](#).
3. Values based on design simulation, not tested in production.

Figure 26. I/O AC characteristics definition



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5.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 29](#)).

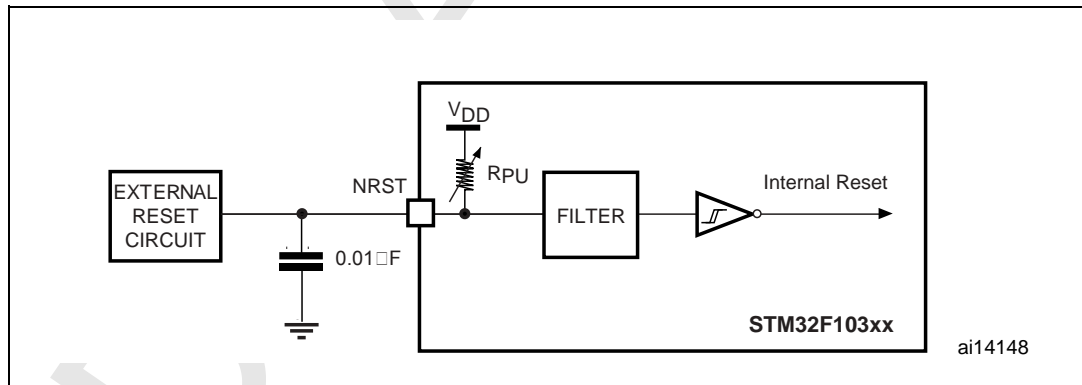
Unless otherwise specified, the parameters given in [Table 32](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 6](#).

Table 32. NRST pin characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ ⁽²⁾	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage ⁽²⁾					V
$V_{IH(NRST)}$	NRST Input high level voltage ⁽²⁾					
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis ⁽³⁾					
R_{PU}	Weak pull-up equivalent resistor ⁽⁴⁾	$V_{IN}=V_{SS}$	TBD	40	TBD	k Ω
$V_{F(NRST)}$	NRST Input filtered pulse ⁽⁵⁾					ns
$V_{NF(NRST)}$	NRST Input not filtered pulse ⁽⁵⁾					μ s

1. TBD stands for To Be Defined.
2. Values based on characterization results, and not tested in production.
3. Hysteresis voltage between Schmitt trigger switching lines.
4. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
5. Values guaranteed by design, not tested in production.

Figure 27. Recommended NRST pin protection



2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 32](#). Otherwise the reset will not be taken into account by the device.

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5.3.14 TIM timer characteristics

Unless otherwise specified, the parameters given in [Table 33](#) are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 6](#).

Refer to [Section 5.3.12: I/O port pin characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 33. TIM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time		2			t_{CK_TIM}
$t_{res(TIM)}$	Timer resolution time					t_{PCLK2}
		$f_{PCLKx} = 10\text{ MHz}$				ns
f_{EXT}	Timer external clock frequency	f_{PCLKx}				MHz
						MHz
Res_{TIM}	Timer resolution			16		bit
$t_{COUNTER}$	16-bit Counter clock period when internal clock is selected					t_{PCLK}
		$f_{PCLKx} = 10\text{ MHz}$				μs
T_{MAX_COUNT}	Maximum Possible Count					t_{PCLK}
		$f_{PCLKx} = 10\text{ MHz}$				s

5.3.15 Communications interfaces

I²C interface characteristics

Unless otherwise specified, the parameters given in [Table 34](#) are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 6](#).

The Root Part Number 1 and Root Part Number 2 I²C interface meets the requirements of the standard I²C communication protocol. The characteristics are described in the [Table 34](#). Refer to [Section 5.3.12: I/O port pin characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

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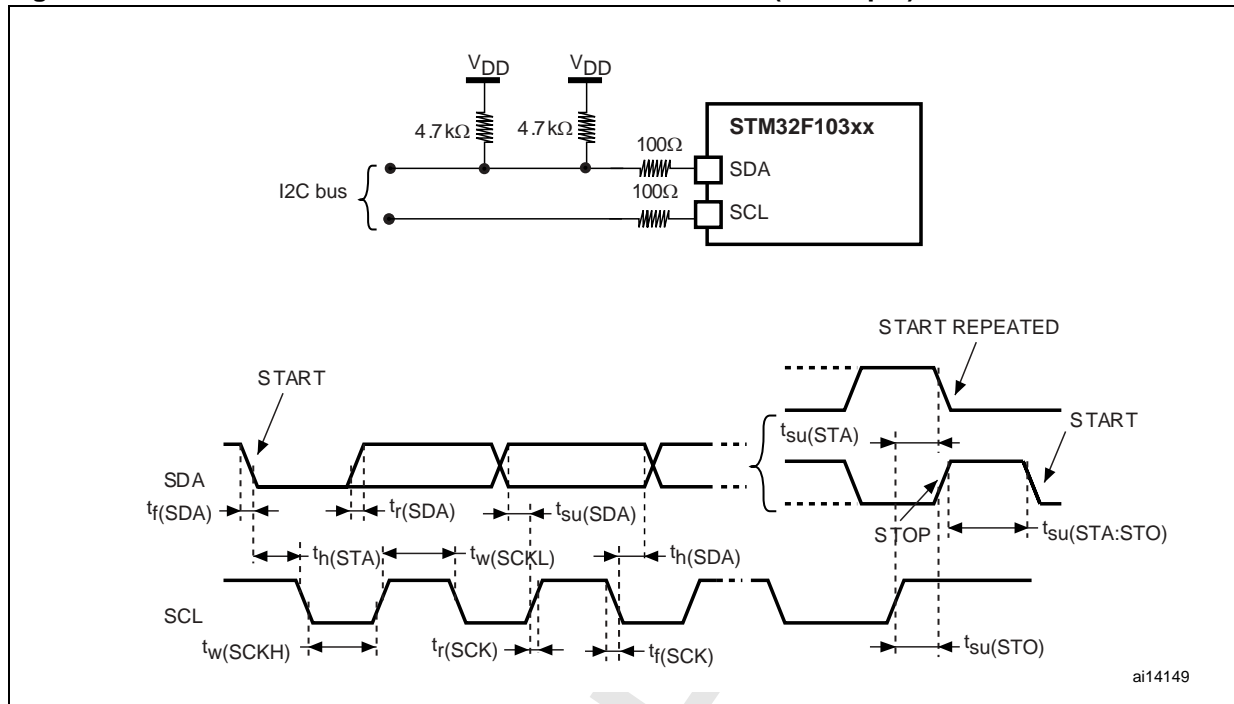
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Table 34. I2C Characteristics

Symbol	Parameter	Standard mode I ² C ⁽¹⁾		Fast mode I ² C ⁽¹⁾⁽²⁾		Unit
		Min	Max	Min	Max	
t _w (SCLL)	SCL clock low time	4.7		1.3		μs
t _w (SCLH)	SCL clock high time	4.0		0.6		
t _{su} (SDA)	SDA setup time	250		100		ns
t _h (SDA)	SDA data hold time	0 ⁽³⁾		0 ⁽⁴⁾	900 ⁽³⁾	
t _r (SDA) t _r (SCL)	SDA and SCL rise time		1000	20+0.1C _b	300	
t _f (SDA) t _f (SCL)	SDA and SCL fall time		300	20+0.1C _b	300	
t _h (STA)	START condition hold time	4.0		0.6		μs
t _{su} (STA)	Repeated START condition setup time	4.7		0.6		
t _{su} (STO)	STOP condition setup time	4.0		0.6		μs
t _w (STO:STA)	STOP to START condition time (bus free)	4.7		1.3		μs
C _b	Capacitive load for each bus line		400		400	pF

1. Values based on standard I²C protocol requirement, not tested in production.
2. f_{PCLK1}, must be at least 8MHz to achieve max fast I²C speed (400kHz).
3. The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 28. I²C bus AC waveforms and measurement circuit (to be split)



1. Measurement points are done at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

Table 35. SCL frequency table ($f_{PCLKx}=10\text{ MHz.}, V_{DD} = 3.3\text{ V}$)⁽¹⁾⁽²⁾⁽³⁾

f _{SCL} (kHz)	I2C_CCR Value
	R _p =4.7kΩ
400	TBD
300	TBD
200	TBD
100	TBD
50	TBD
20	TBD

1. TBD = To Be Defined.
2. R_p = External pull-up resistance, f_{SCL} = I²C speed,
3. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

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SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 36](#) are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 6](#).

Refer to [Section 5.3.12: I/O port pin characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 36. SPI characteristics⁽¹⁾

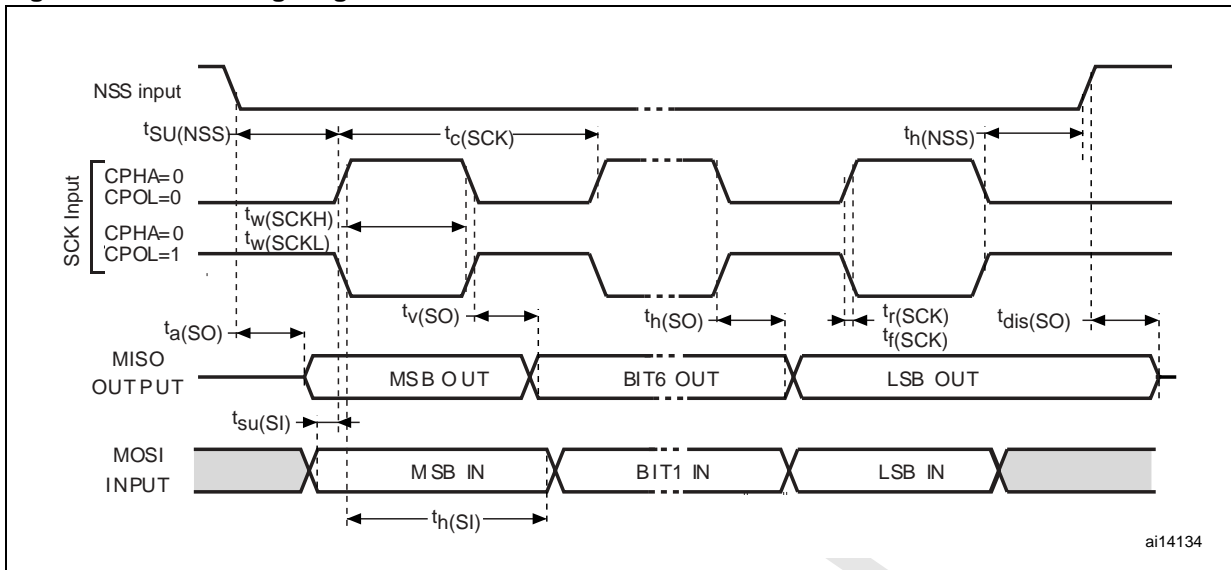
Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_c(SCK)$	SPI clock frequency	Master mode	TBD	TBD	MHz
		Slave mode	0	TBD	
$t_r(SCK)$ $t_f(SCK)$	SPI clock rise and fall time	Capacitive load: C=50 pF		TBD	ns
$t_{su(NSS)}^{(2)}$	NSS setup time	Slave mode	0		
$t_{h(NSS)}^{(2)}$	NSS hold time	Slave mode	0		
$t_w(SCKH)^{(2)}$ $t_w(SCKL)^{(2)}$	SCK high and low time	Master mode, $f_{PCLK} = TBD$, presc = TBD	TBD		
$t_{su(MI)}^{(2)}$ $t_{su(SI)}^{(2)}$	Data input setup time	Master mode	TBD		
		Slave mode	TBD		
$t_{h(MI)}^{(2)}$ $t_{h(SI)}^{(2)}$	Data input hold time	Master mode	TBD		
		Slave mode	TBD		
		Master mode, $f_{PCLK} = TBD$	TBD ⁽³⁾		
		Slave mode, $f_{PCLK} = TBD$	TBD ⁽³⁾		
$t_{a(SO)}^{(2)(4)}$	Data output access time	Slave mode	TBD	TBD	
		Slave mode, $f_{PCLK} = TBD$	TBD	TBD	
$t_{dis(SO)}^{(2)(5)}$	Data output disable time	Slave mode	TBD	TBD	
$t_{v(SO)}^{(2)(1)}$	Data output valid time	Slave mode (after enable edge)		TBD	
		$f_{PCLK} = TBD$		TBD	
$t_{v(MO)}^{(2)(1)}$	Data output valid time	Master mode (after enable edge)		TBD	
		$f_{PCLK} = TBD$	TBD	TBD	
$t_{h(SO)}^{(2)}$ $t_{h(MO)}^{(2)}$	Data output hold time	Slave mode (after enable edge)	TBD		
		Master mode (after enable edge)	TBD		

1. TBD = To Be Defined.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Depends on f_{PCLK} . For example, if $f_{PCLK} = 8MHz$, then $t_{PCLK} = 1/f_{PCLK} = 125 ns$ and $t_{v(MO)} = 255 ns$.
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

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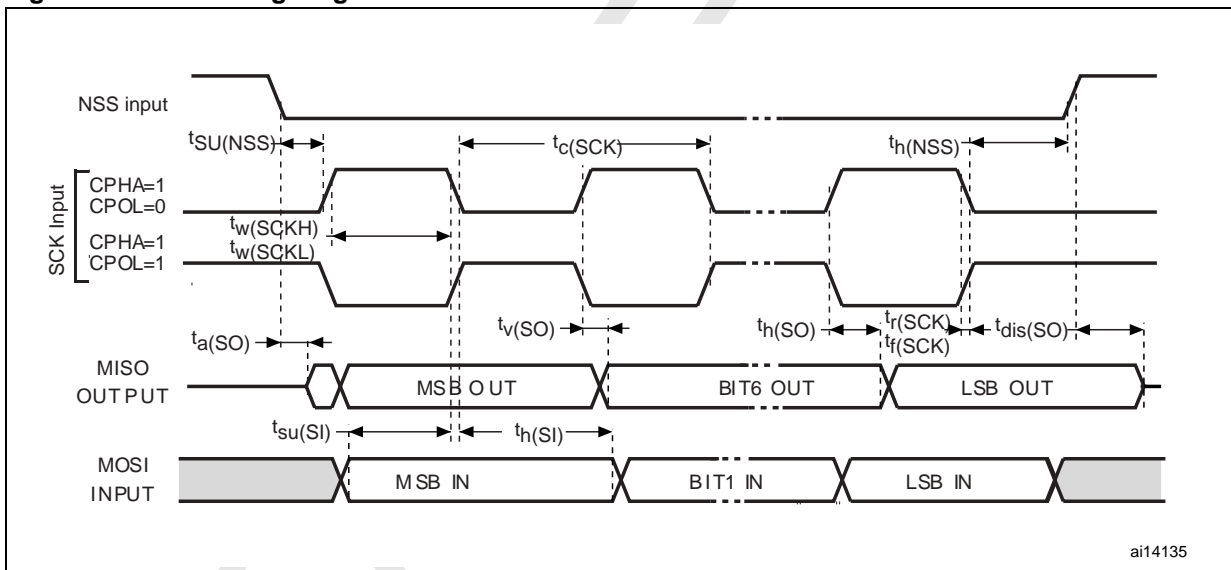
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Figure 29. SPI timing diagram - slave mode and CPHA=0



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

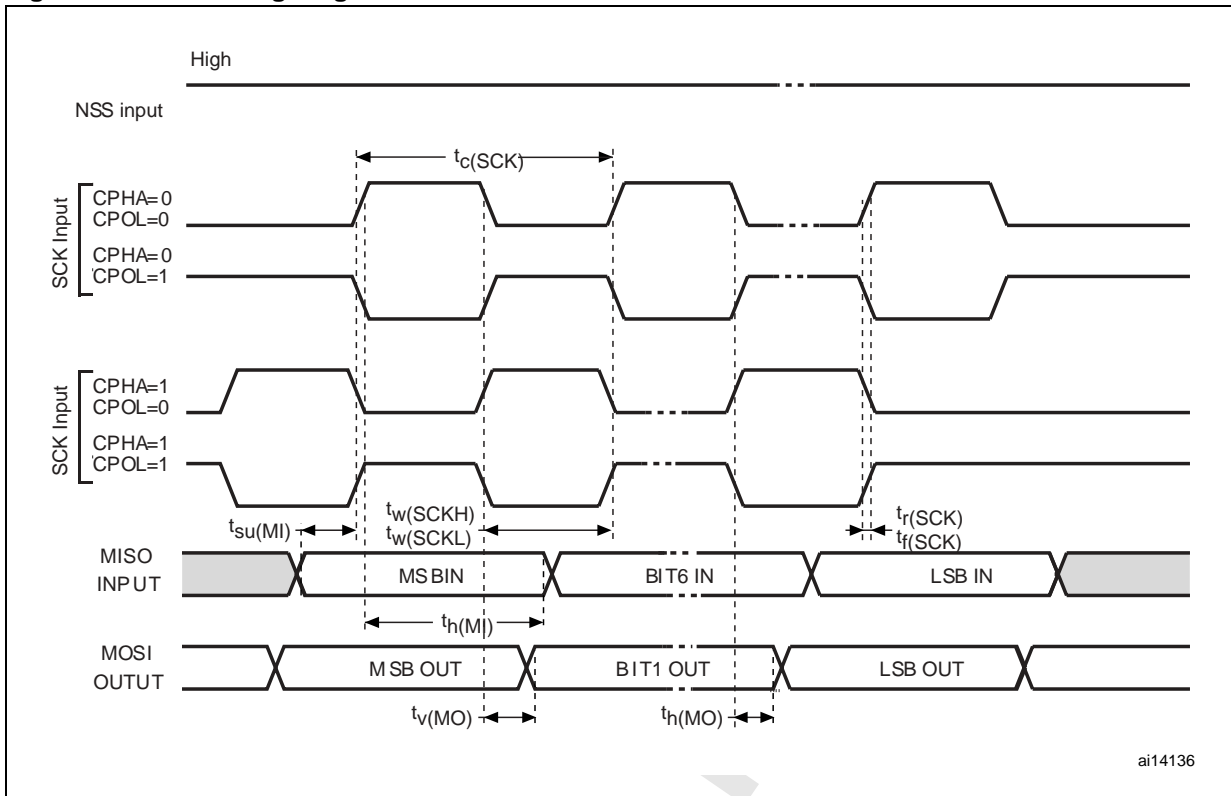
Figure 30. SPI timing diagram - slave mode and CPHA=1¹⁾



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Figure 31. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

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USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 37. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min. ⁽¹⁾⁽²⁾	Max. ⁽¹⁾⁽²⁾	Unit
Input Levels					
V_{DI}	Differential Input Sensitivity	I(USBDP, USBDM)	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	
V_{SE}	Single Ended Receiver Threshold		1.3	2.0	
Output Levels					
V_{OL}	Static Output Level Low	R_L of 1.5 k Ω to 3.6 V ⁽³⁾		0.3	V
V_{OH}	Static Output Level High	R_L of 15 k Ω to V_{SS} ⁽³⁾	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. It is important to be aware that the USBDP/USBDM pins are not 5 V tolerant. As a consequence, in case of a shortcut with V_{bus} (typ value = 5.0 V), the protection diodes of the USBDP/USBDM pins will be direct biased. This will not damage the device if not more than 50 mA is sunk for longer than 24 hours but the reliability may be affected.
3. R_L is the load connected on the USB drivers

Figure 32. USB timings: definition of data signal rise and fall time

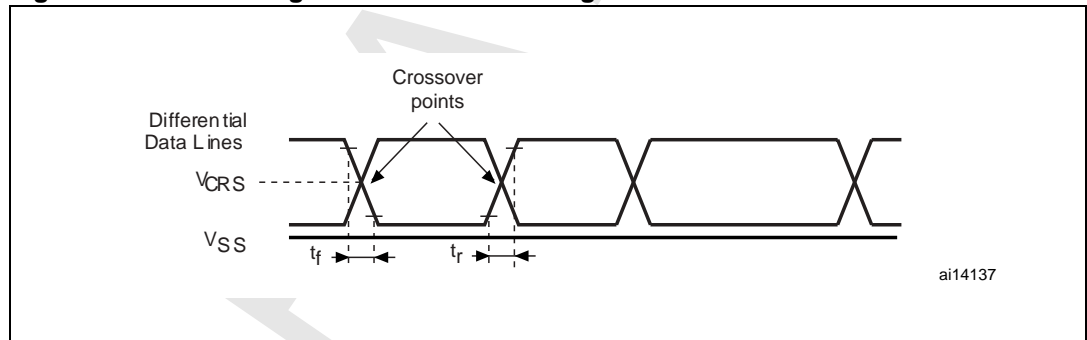


Table 38. USB: Full speed electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Driver characteristics					
t_r	Rise time ⁽¹⁾	$C_L=50$ pF	4	20	ns
t_f	Fall Time ⁽¹⁾	$C_L=50$ pF	4	20	ns
t_{rfm}	Rise/ Fall Time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal Crossover Voltage		1.3	2.0	V

1. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

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5.3.16 CAN - Controller Area Network Interface

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (CANTX and CANRX).

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 39](#) are derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 6](#).

Table 39. ADC characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ ¹⁾	Max	Unit
V_{DDA}	ADC power supply		2.4V		3.6V	V
V_{REF+}	Positive Reference Voltage		TBD		V_{DDA}	V
f_{ADC}	ADC clock frequency		0.6		14	MHz
f_S	Sampling rate	TBD	0.05		1	MHz
V_{AIN}	Conversion voltage range ²⁾		V_{SSA}		V_{DDA}	V
R_{AIN}	External input impedance		TBD ⁽²⁾⁽³⁾			k Ω
C_{AIN}	External capacitor on analog input					pF
I_{lkg}	Negative input leakage current on analog pins	$V_{IN} < V_{SS}, I_{IN} < 400\mu A$ on adjacent analog pin		5	6	μA
R_{ADC}	Sampling switch resistance				1	k Ω
C_{ADC}	Internal sample and hold capacitor				5	pF
t_{CAL}	Calibration time	$f_{ADC} = 14\text{MHz}$	5.9			μs
			83			$1/f_{ADC}$
$t_S^{(2)}$	Sampling time	$f_{ADC} = 14\text{MHz}$	0.107		17.1	μs
t_{CONV}	Total conversion time (including sampling time)	$f_{ADC} = 14\text{MHz}$	1		18	μs
			14 (1.5 for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. TBD = To Be Defined.

2. Depending on the input signal variation (f_{AIN}), C_{AIN} can be increased for stabilization time and reduced to allow the use of a larger serial resistor (R_{AIN}). It is valid for all f_{ADC} frequencies ≤ 14 MHz.

3. During the sample time the input capacitance C_{AIN} (5 max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S . After the end of the sample time t_S , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

Table 40. ADC accuracy with $f_{PCLK2} = 10\text{MHz}$, $f_{ADC} = 10\text{MHz}$, $R_{AIN} < 10\text{k}\Omega$, $V_{DDA} = 3.3\text{V}$.
(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$ E_T $	Total unadjusted error ⁽²⁾		TBD	TBD	LSB
$ E_O $	Offset error ⁽²⁾		TBD	TBD	
$ E_G $	Gain Error ⁽²⁾		TBD	TBD	
$ E_D $	Differential linearity error ⁽²⁾		TBD	TBD	
$ E_L $	Integral linearity error ⁽²⁾		TBD	TBD	

1. TBD = To Be Defined.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 5.3.12](#) does not affect the ADC accuracy.

Figure 33. ADC accuracy characteristics

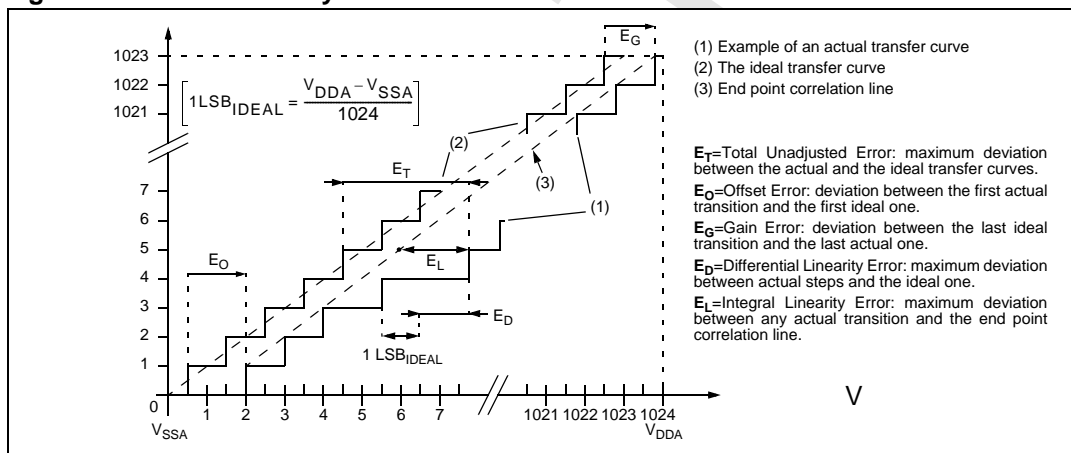
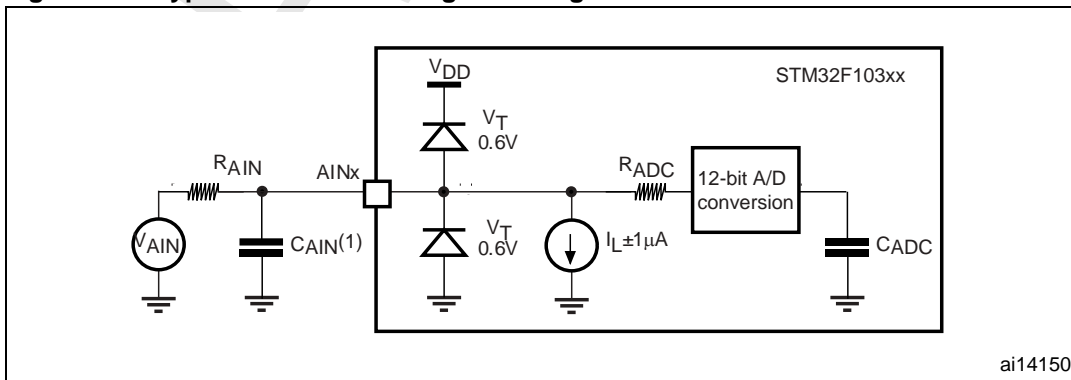


Figure 34. Typical connection diagram using the ADC



1. Refer to [Table 39](#) for the values of R_{ADC} and C_{ADC} .
2. $C_{PARASITIC}$ must be added to C_{AIN} . It represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3 pF). A high $C_{PARASITIC}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

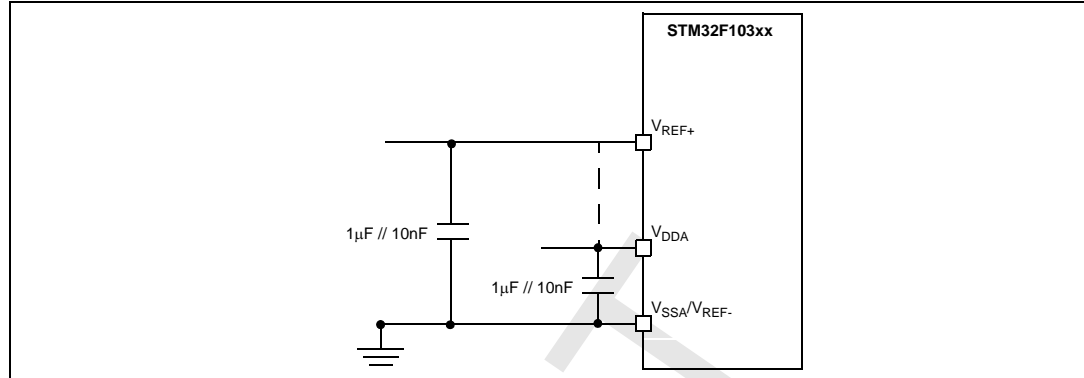
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General PCB design guidelines

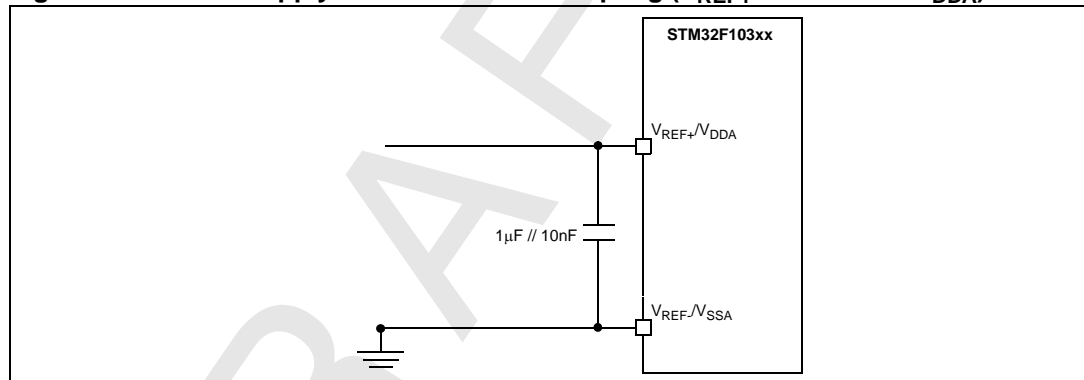
Power supply decoupling should be performed as shown in *Figure 35* or *Figure 36*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 35. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. VREF+ and VREF- inputs are available only on 100-pin packages.

Figure 36. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. VREF+ and VREF- inputs are available only on 100-pin packages.

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5.3.18 Temperature sensor characteristics

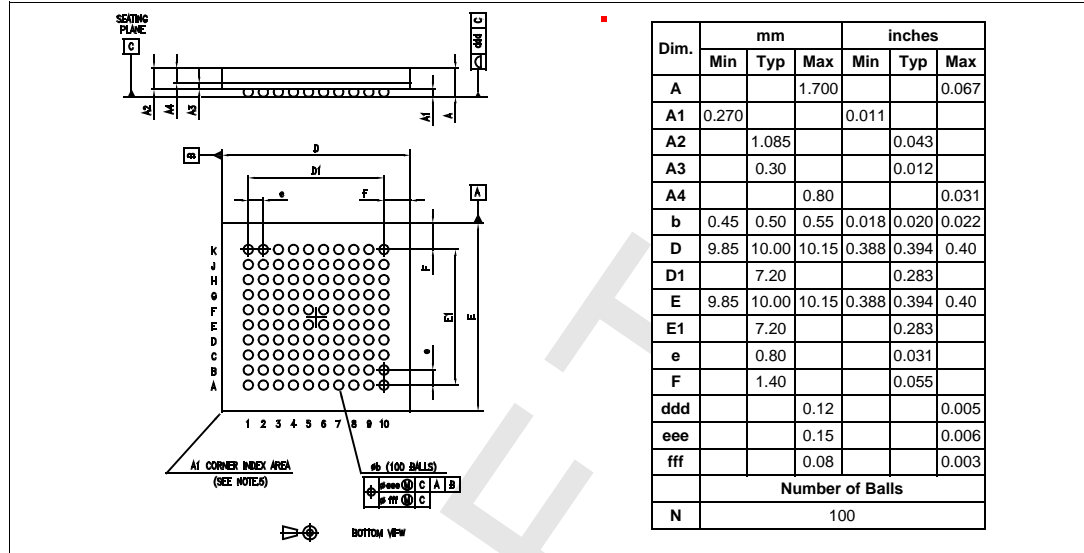
Table 41. TS characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature			± 1.5		$^{\circ}C$
Avg_Slope	Average slope			4.478		$mV/^{\circ}C$
V_{25}	Voltage at 25 $^{\circ}C$			TBD		V
t_{START}	Startup time		4		10	μs

6 Package characteristics

6.1 Package Mechanical Data

Figure 37. 100-Low Profile Fine Pitch Ball Grid Array Package



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Figure 38. Recommended PCB Design rules (0.80/0.75mm pitch BGA)

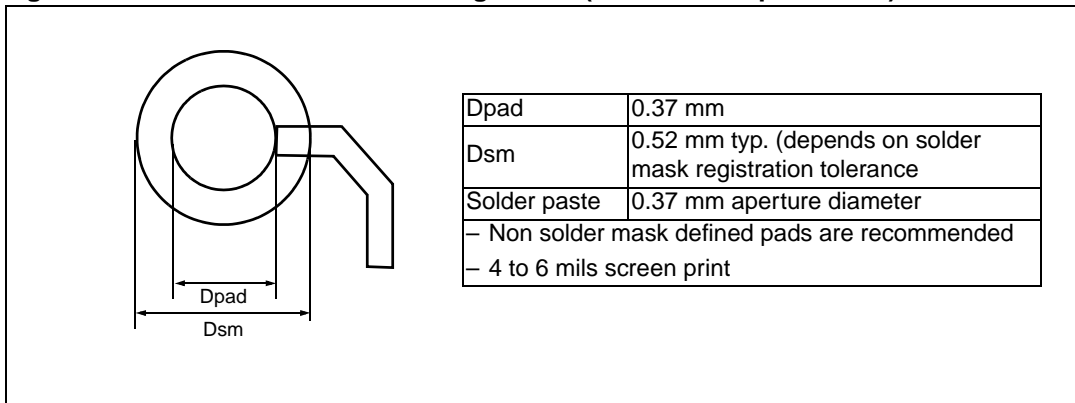


Figure 39. 100-Pin Low-profile Quad Flat Package

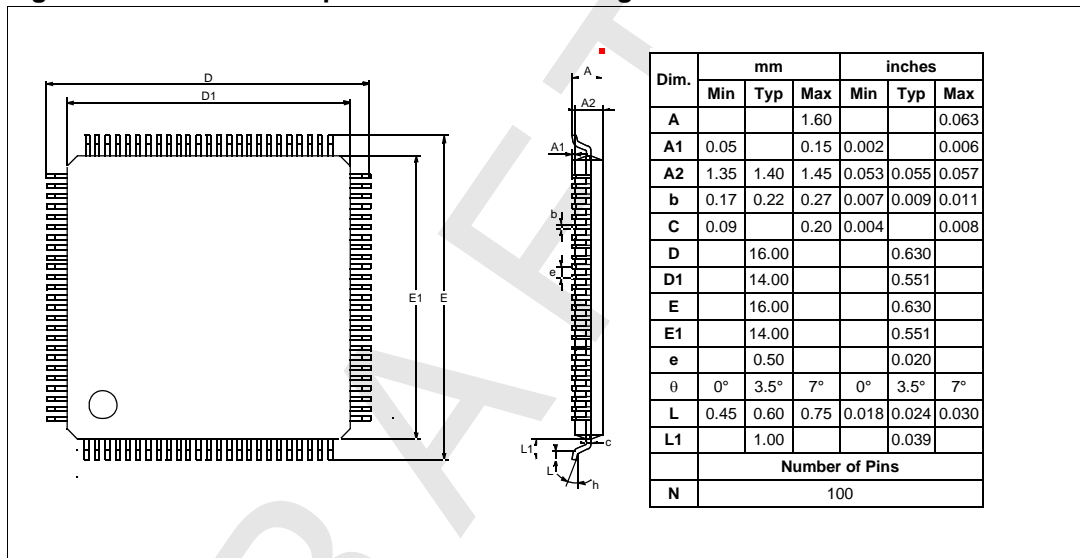
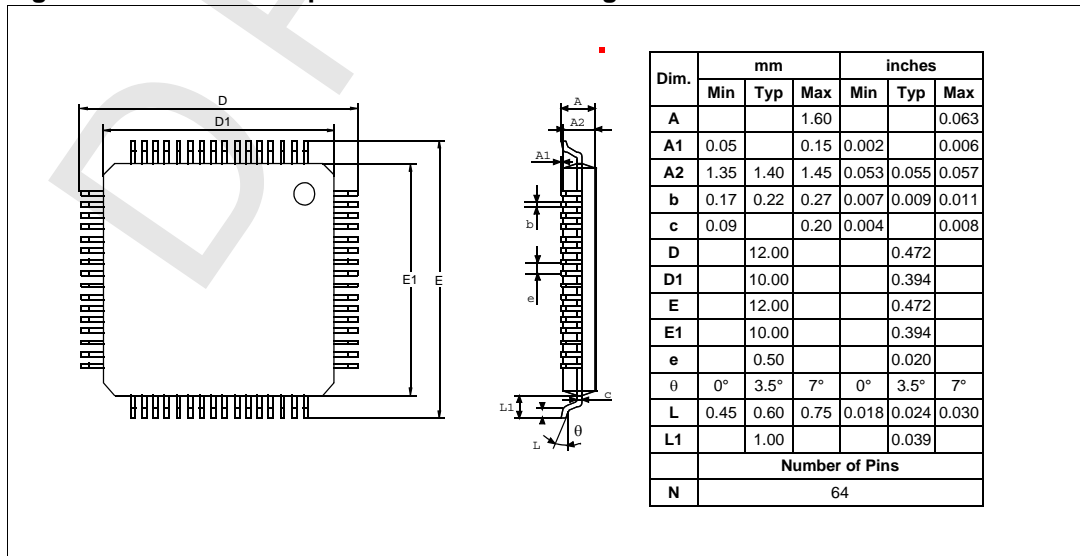


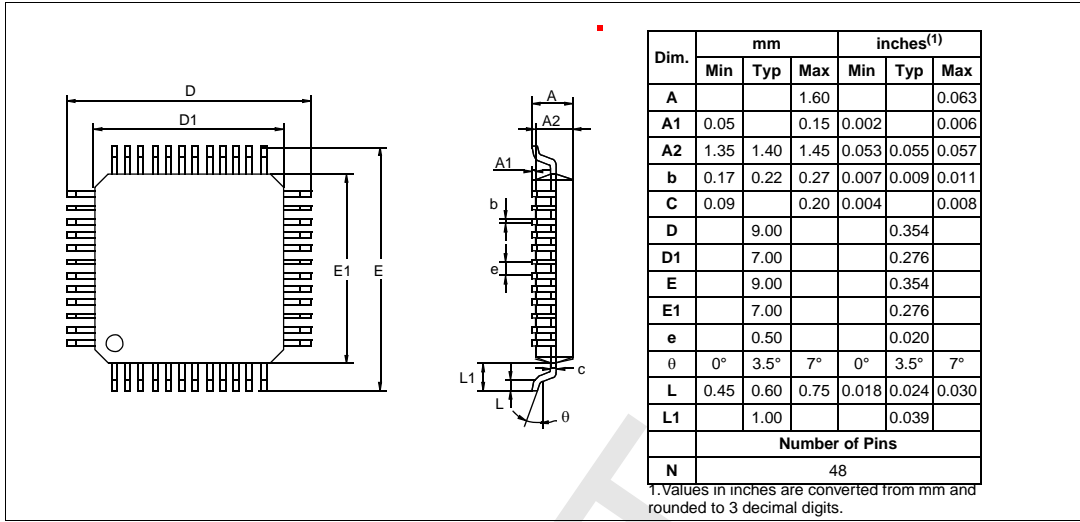
Figure 40. 64-Pin Low-profile Quad Flat Package



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Figure 41. 48-Pin Low-profile Quad Flat Package



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6.2 Thermal characteristics

The average chip-junction temperature, T_J , in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD} , expressed in Watts. This is the Chip Internal Power.

$P_{I/O}$ represents the Power Dissipation on Input and Output Pins;

Most of the time for the application $P_{I/O} < P_{INT}$ and can be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273 \text{ °C}) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273\text{°C}) + \Theta_{JA} \times P_D^2 \quad (3)$$

where:

K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A .

Table 42. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal Resistance Junction-Ambient LFBGA100 - 10 x 10 mm / 0.5 mm pitch	41	°C/W
	Thermal Resistance Junction-Ambient LQFP 100 - 14 x 14 mm / 0.5 mm pitch	46	
	Thermal Resistance Junction-Ambient LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	
	Thermal Resistance Junction-Ambient LQFP 48 - 7 x 7 mm / 0.5 mm pitch	TBD	

7 Order codes

Table 43. Order codes

Partnumber	Flash Prog. Memory Kbytes	SRAM Memory Kbytes	Package
STM32F10MC6T6	32	6	LQFP48
STM32F103C6T6		10	
STM32F103C8T6	64	20	
STM32F10MR6T6	32	6	LQFP64
STM32F103R6T6		10	
STM32F103R8T6	64	20	
STM32F103RBT6	128	20	
STM32F103V8T6	64	20	LQFP100
STM32F103VBT6	128	20	
STM32F103V8H6	64	20	LFBGA100
STM32F103VBH6	128	20	

7.1 Future family enhancements

Further developments of the STM32F103 Performance Line will see an expansion of the current options. Larger packages will soon be available with up to 512KB Flash, 64KB SRAM and with extended features such as EMI support, SDIO, I2S, DAC and additional timers and USARTS.

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8 Revision history

Table 44. Document revision history

Date	Target Revision	Draft Revision	Changes
xx-xxx-2007	1	0.1	Initial release.

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DRAFT

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