

REVISION HISTORY				
ZONE	REV	DESCRIPTION	DATE	APPROVED

GALILEO

INTEL QUARK X1000

FAB D

PB: G87173-204

PBA: G87171-400

LB1



WEEE

LB6V1



1500X500_TARGET
SERIAL NUMBER

LB3



1375X250_TARGET
MAC ADDRESS LABEL

DRAWN BY	DATE	INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		
APPROVED BY	DATE			
TITLE		DOCUMENT NUMBER	REV	
GALILEO		G87171	1.0	
SHEET 1 OF 27				

TABLE OF CONTENTS

SHEET NUMBER	SHEET NAME	SHEET NUMBER	SHEET NAME
1	TITLE PAGE		
2	TABLE OF CONTENTS		
3	DISCLAIMER		
4	SYSTEM BLOCK DIAGRAM		
5	QUARK DDR3 & PCIE		
6	QUARK GPIO		
7	QUARK MISC		
8	QUARK POWER		
9	QUARK DECOUPLING		
10	SDRAM 1		
11	SDRAM 2		
12	SDRAM TERMINATION		
13	MINI PCIE CONNECTOR		
14	MICRO SD CONNECTOR		
15	USB CONNECTORS		
16	UART 1		
17	LAN		
18	SPI: ADC&FLASH		
19	I2CPROM & JTAG CONN		
20	QUARK STRAPS		
21	EXTERNAL IO MUXING		
22	ANALOG CONNECTOR & MUXES		
23	EXTERNAL IO CONNECTORS		
24	VOLTAGE REGULATORS		
25	VOLTAGE REGULATORS		
26	VOLTAGE REGULATORS		
27	POWER BUTTONS & MISC		

D

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B

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C

C

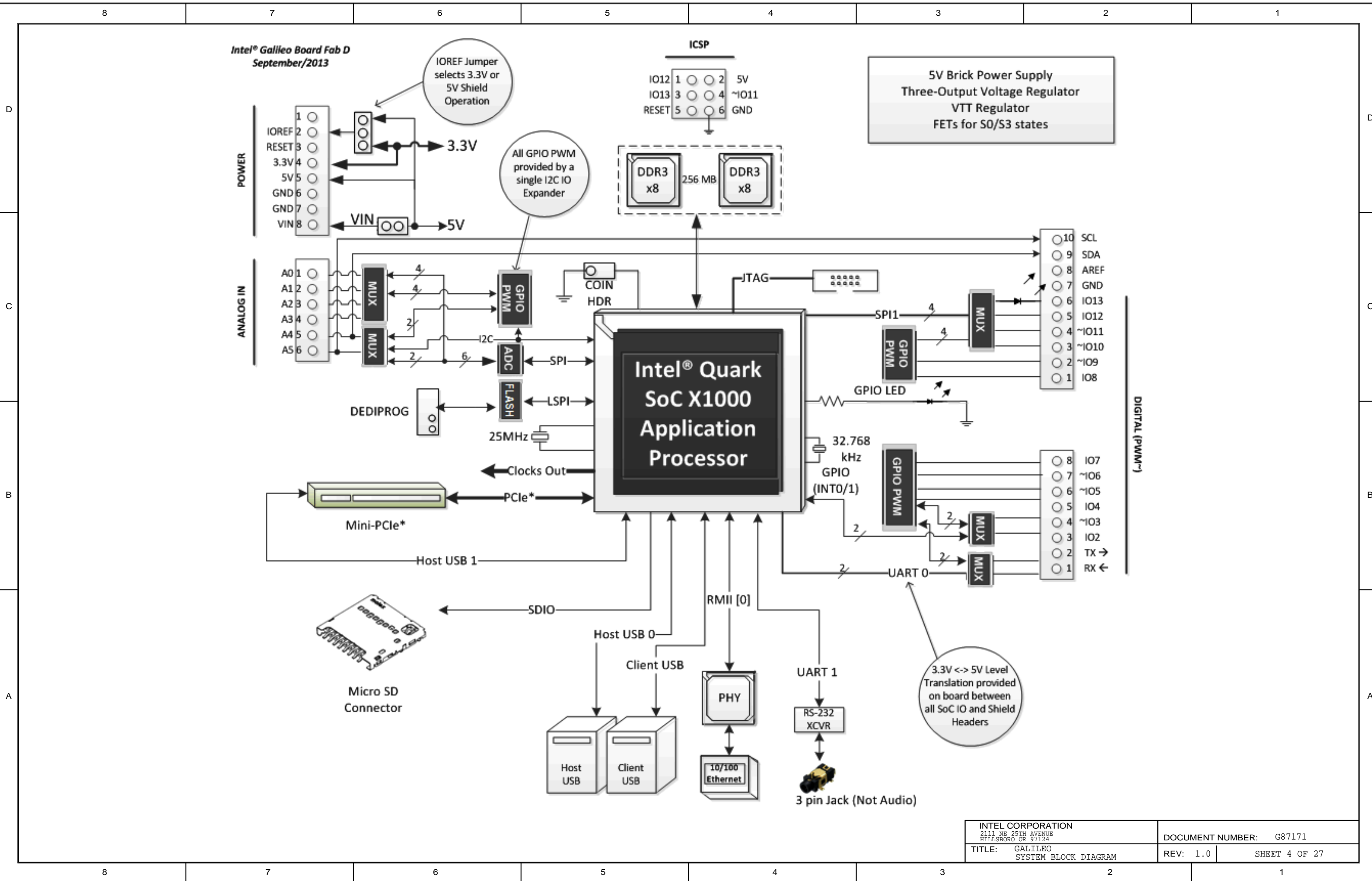
B

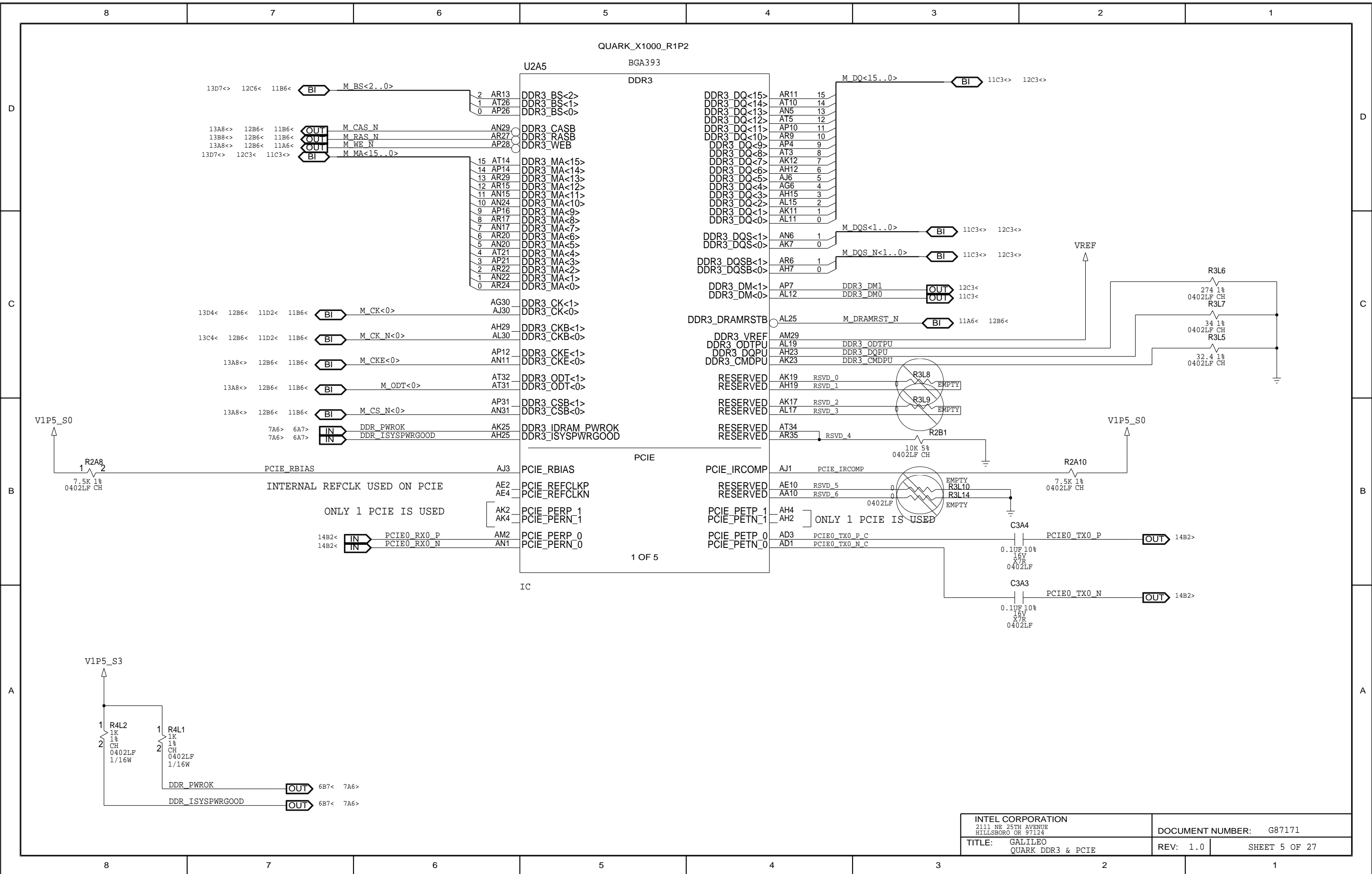
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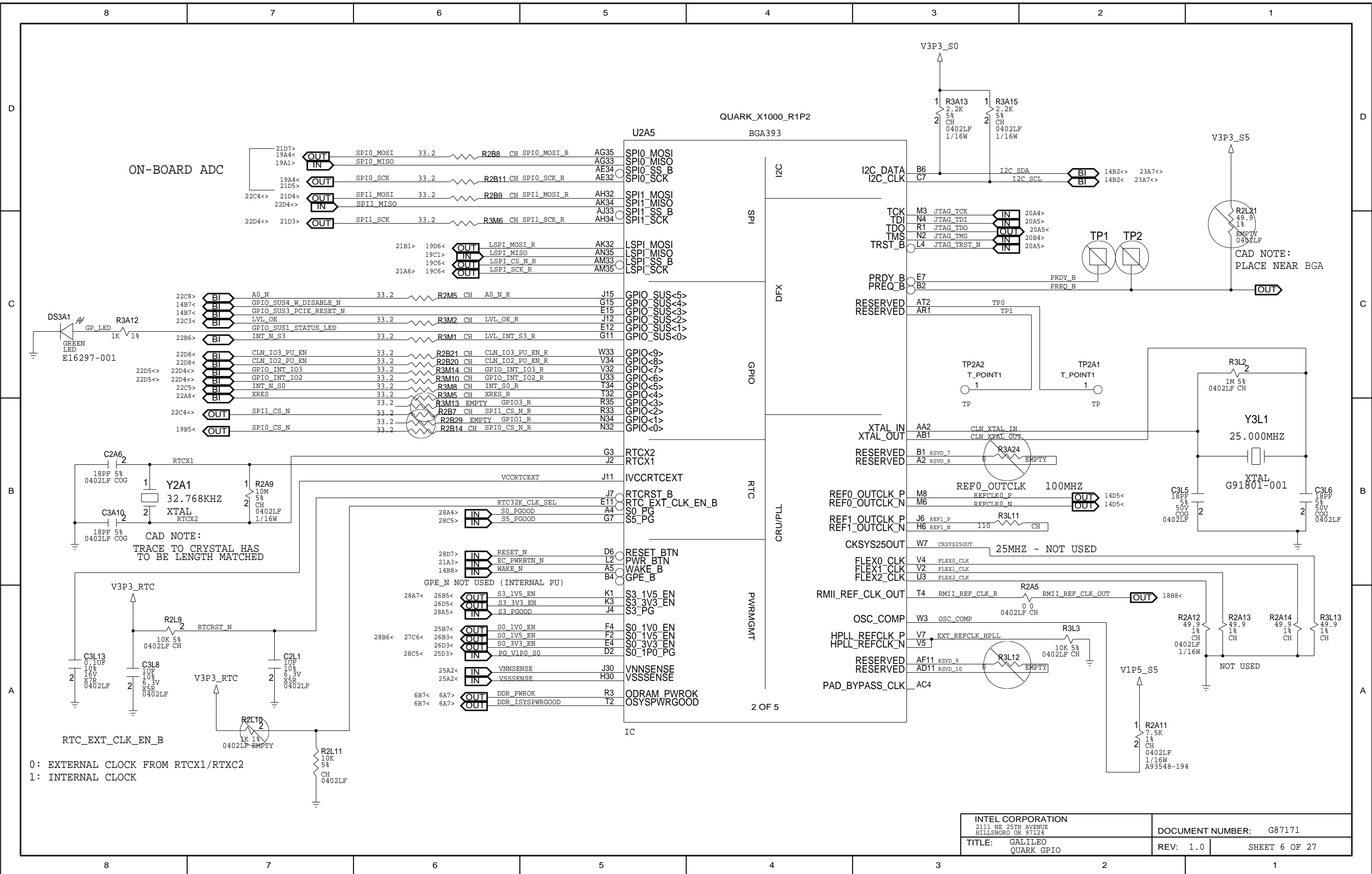
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INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO DISCLAIMER		REV: 1.0	SHEET 3 OF 27

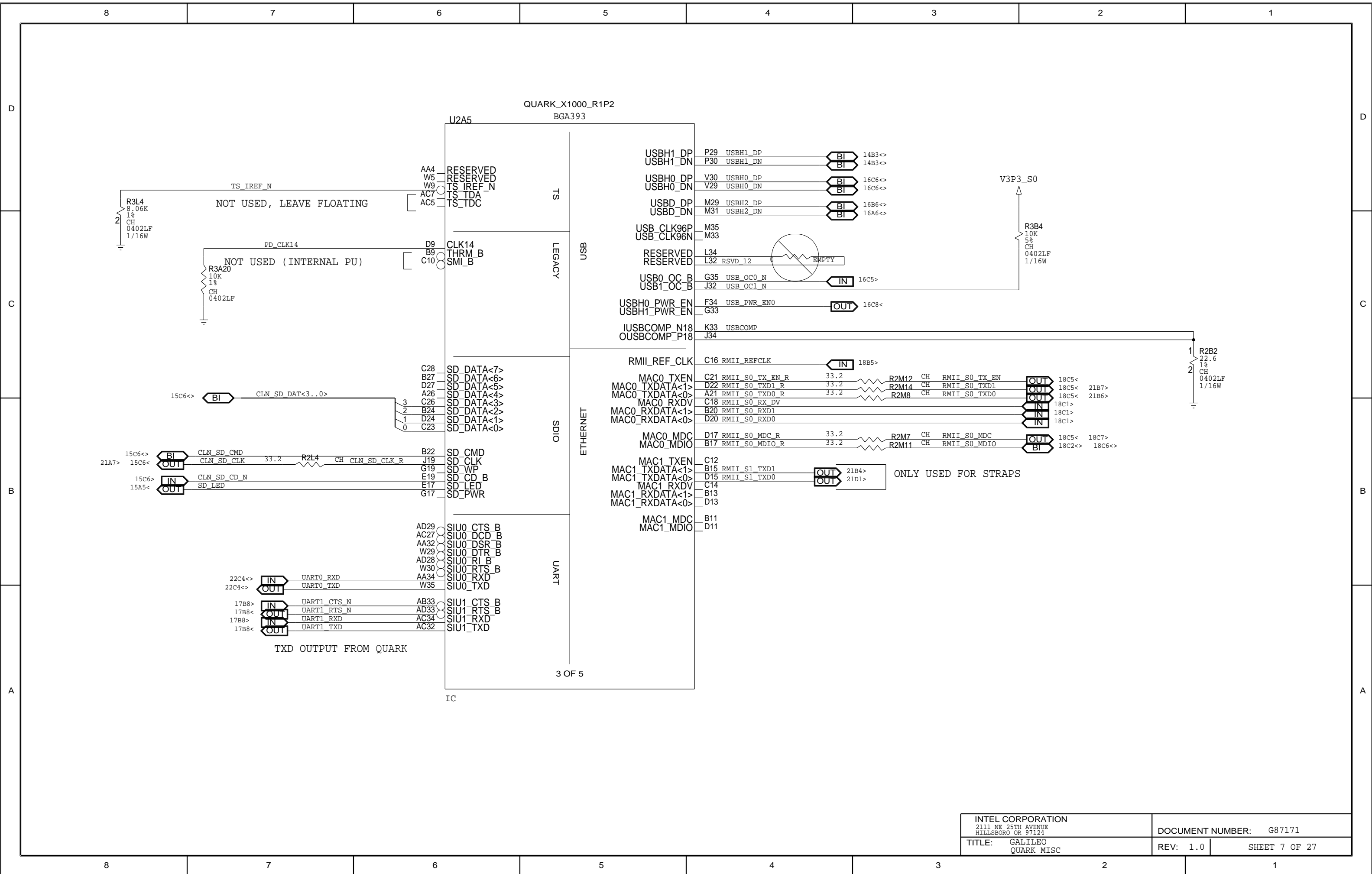


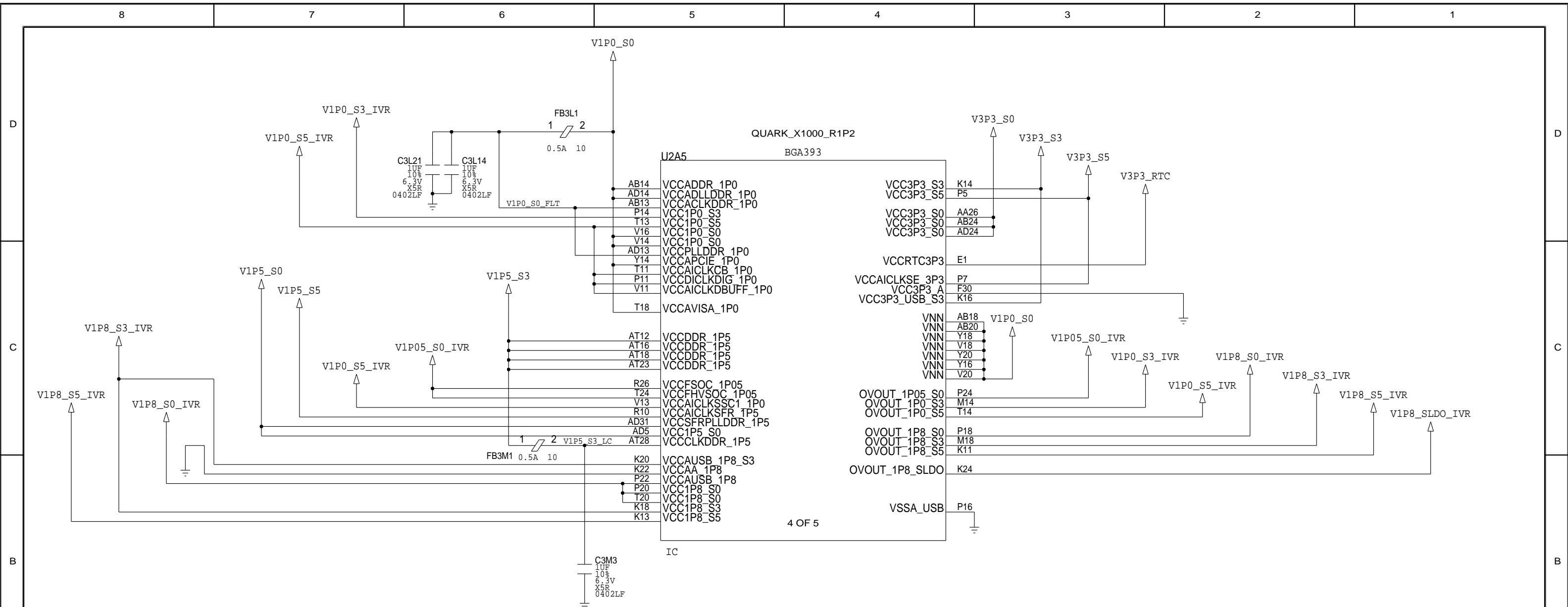




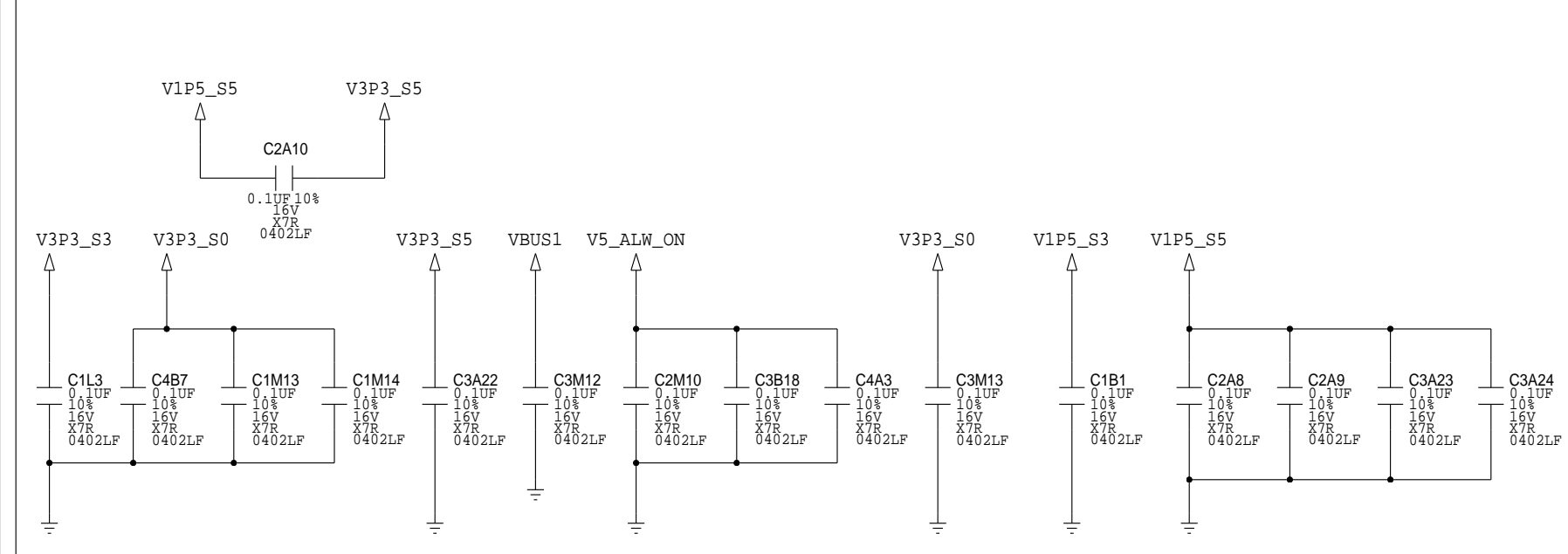
0: EXTERNAL CLOCK FROM RTCX1/RTXC2
 1: INTERNAL CLOCK

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO QUARK GPIO		REV: 1.0	SHEET 6 OF 27



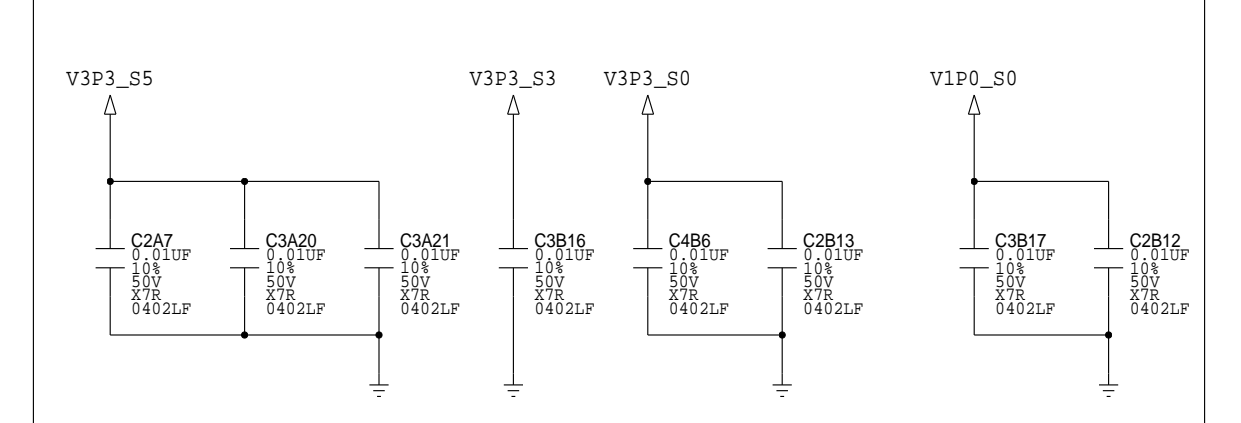


STITCHING CAPS FOR SPLIT PLANES

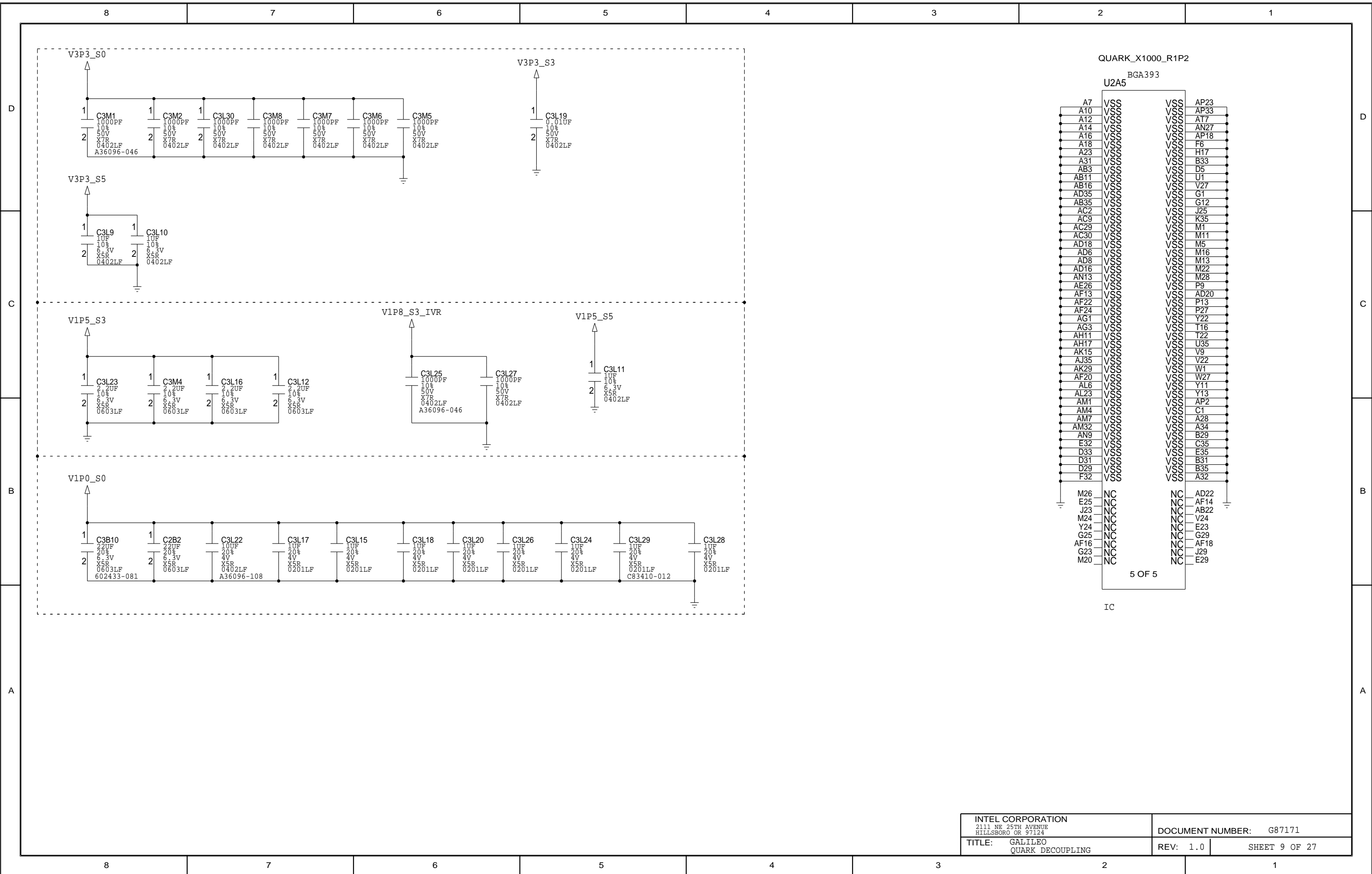


CAD NOTE
PLACE AS CLOSE AS POSSIBLE TO SIGNAL VIAS

STITCHING CAPS FOR SIGNAL REFERENCE TRANSITION



INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO QUARK POWER		REV: 1.0	SHEET 8 OF 27

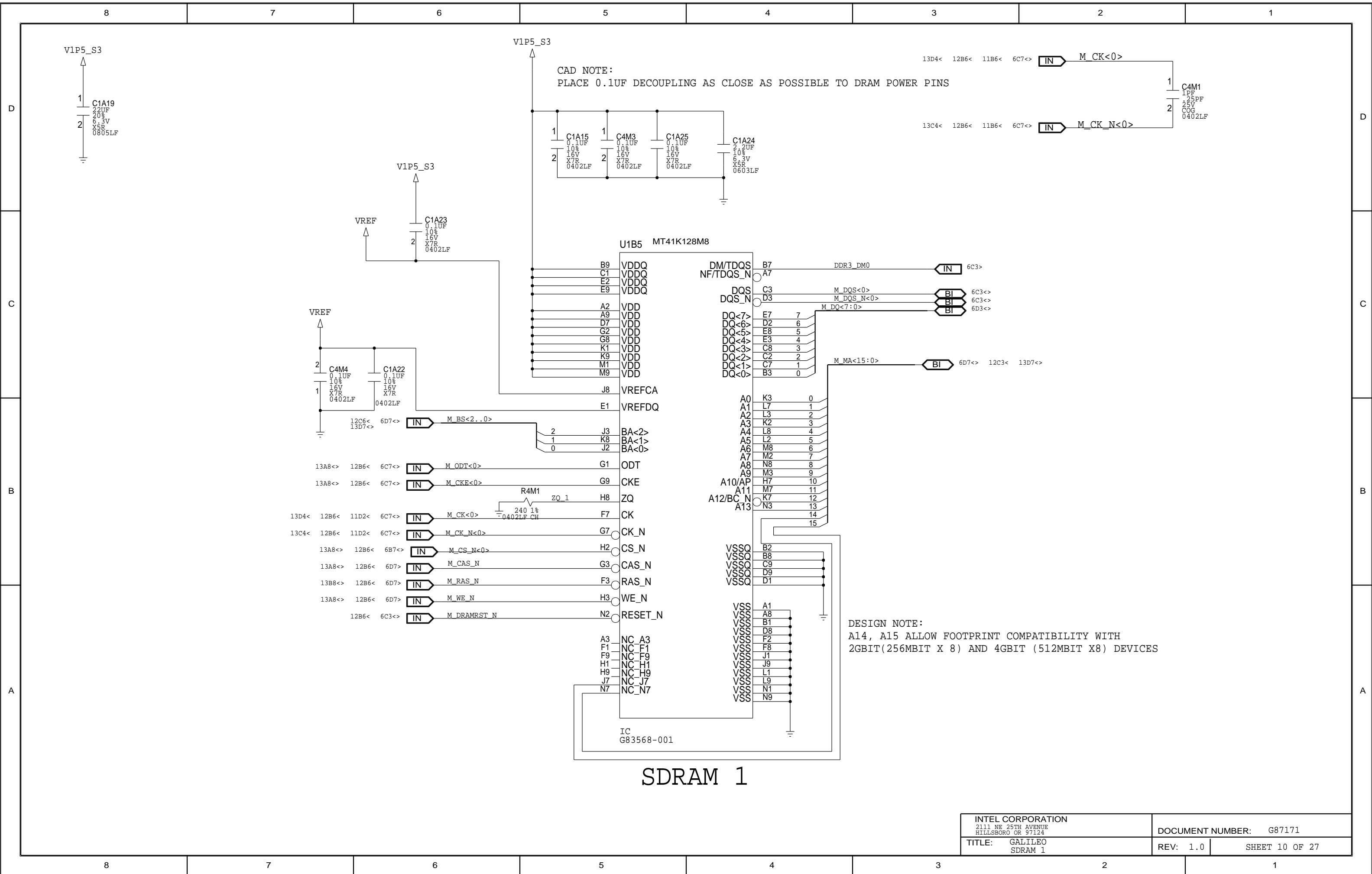


QUARK_X1000_R1P2
BGA393
U2A5

A7	VSS	VSS	AP23
A10	VSS	VSS	AP33
A12	VSS	VSS	AT7
A14	VSS	VSS	AN27
A16	VSS	VSS	AP18
A18	VSS	VSS	F6
A23	VSS	VSS	H17
A31	VSS	VSS	B33
AB3	VSS	VSS	D5
AB11	VSS	VSS	U1
AB16	VSS	VSS	V27
AD35	VSS	VSS	G1
AB35	VSS	VSS	G12
AC2	VSS	VSS	J25
AC9	VSS	VSS	K35
AC29	VSS	VSS	M1
AC30	VSS	VSS	M11
AD18	VSS	VSS	M5
AD6	VSS	VSS	M16
AD8	VSS	VSS	M13
AD16	VSS	VSS	M22
AN13	VSS	VSS	M28
AE26	VSS	VSS	P9
AF13	VSS	VSS	AD20
AF22	VSS	VSS	P13
AF24	VSS	VSS	P27
AG1	VSS	VSS	Y22
AG3	VSS	VSS	T16
AH11	VSS	VSS	T22
AH17	VSS	VSS	U35
AK15	VSS	VSS	V9
AJ35	VSS	VSS	V22
AK29	VSS	VSS	W1
AF20	VSS	VSS	W27
AL6	VSS	VSS	Y11
AL23	VSS	VSS	Y13
AM1	VSS	VSS	AP2
AM4	VSS	VSS	C1
AM7	VSS	VSS	A28
AM32	VSS	VSS	A34
AN9	VSS	VSS	B29
E32	VSS	VSS	C35
D33	VSS	VSS	E35
D31	VSS	VSS	B31
D29	VSS	VSS	B35
F32	VSS	VSS	A32
M26	NC	NC	AD22
E25	NC	NC	AF14
J23	NC	NC	AB22
M24	NC	NC	V24
Y24	NC	NC	E23
G25	NC	NC	G29
AF16	NC	NC	AF18
G23	NC	NC	J29
M20	NC	NC	E29

5 OF 5

IC

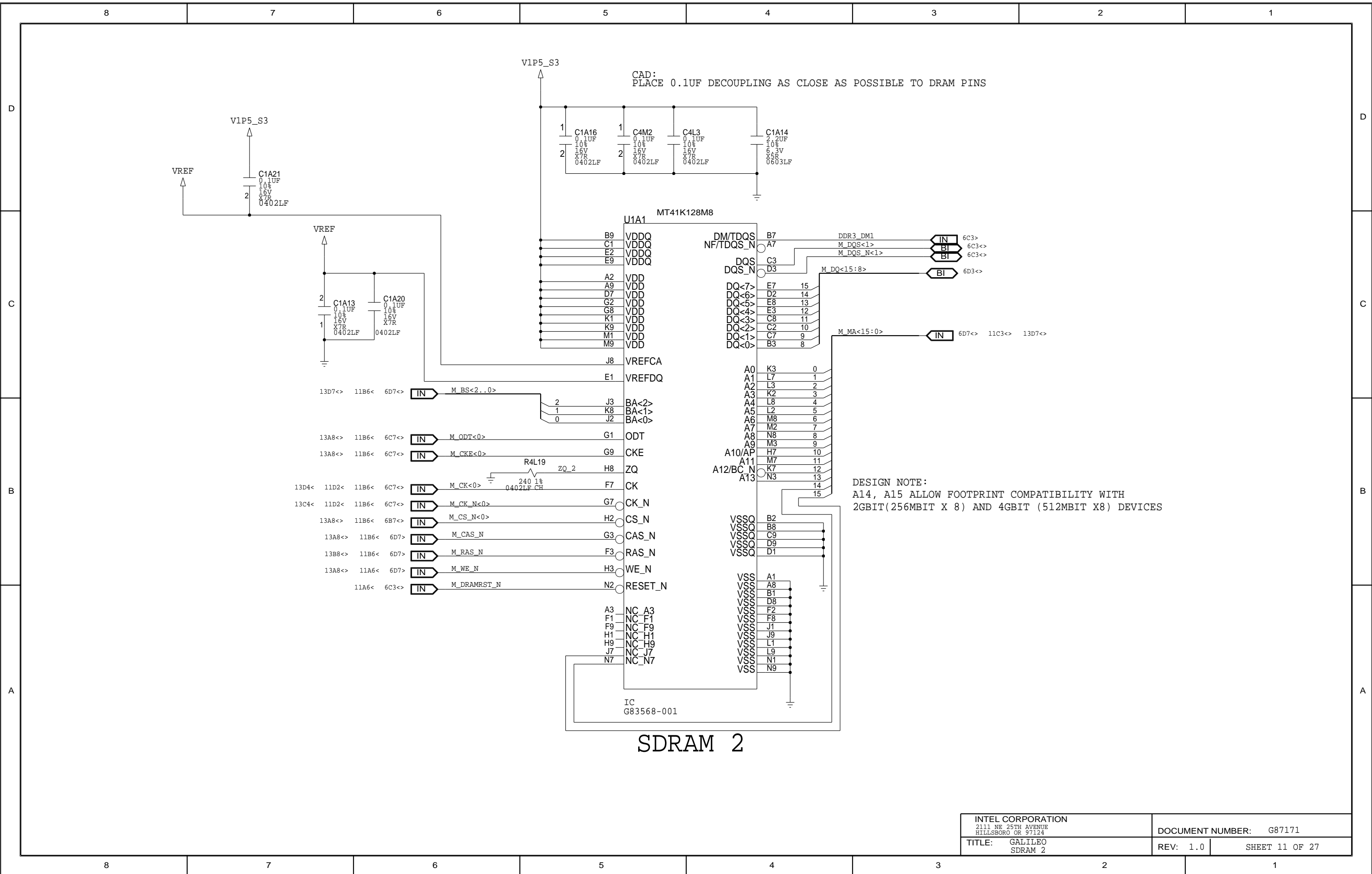


CAD NOTE:
PLACE 0.1UF DECOUPLING AS CLOSE AS POSSIBLE TO DRAM POWER PINS

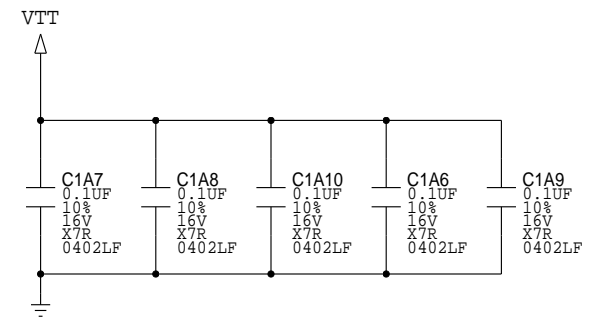
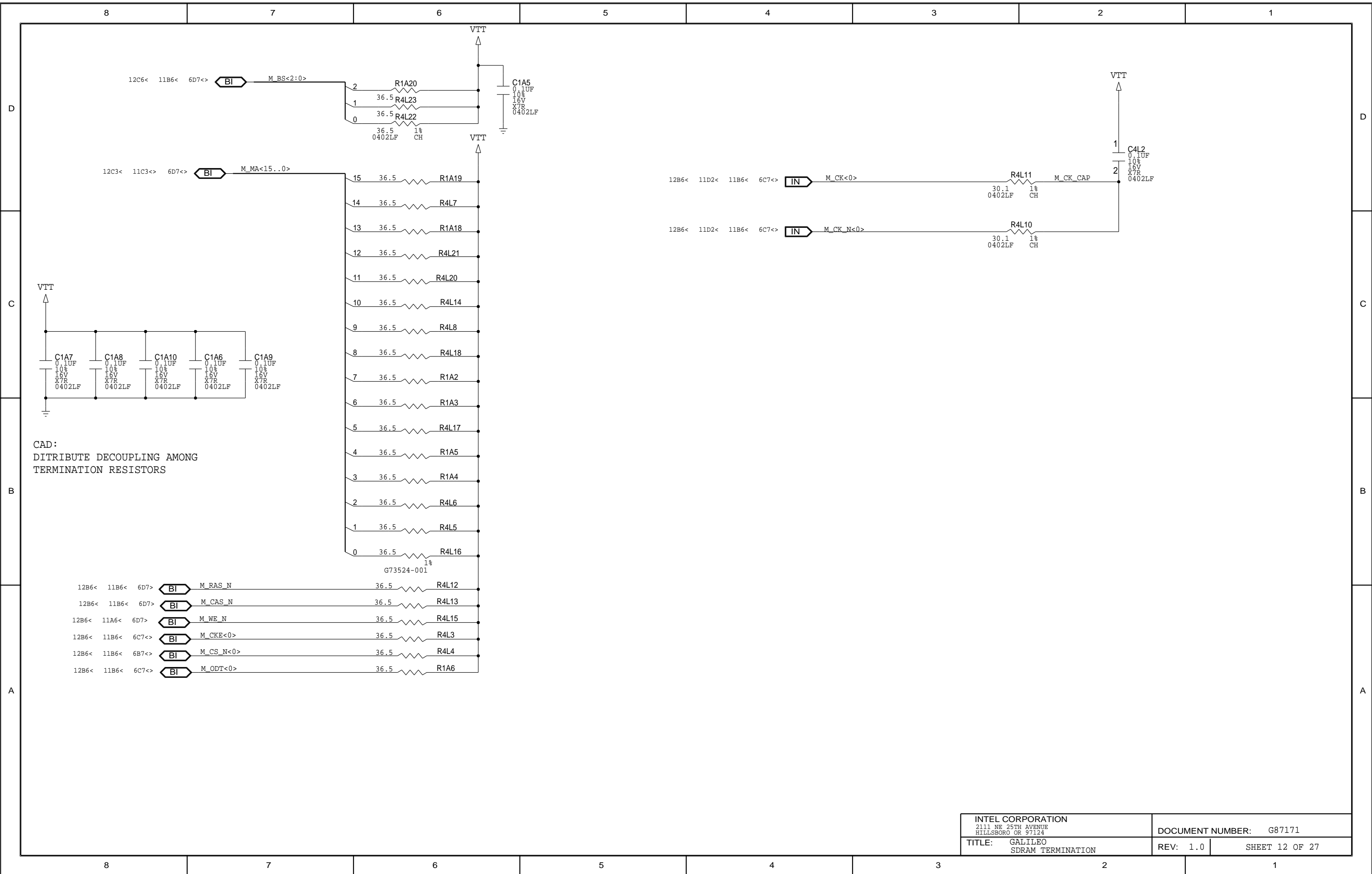
DESIGN NOTE:
A14, A15 ALLOW FOOTPRINT COMPATIBILITY WITH
2GBIT(256MBIT X 8) AND 4GBIT (512MBIT X8) DEVICES

SDRAM 1

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO SDRAM 1		REV: 1.0	SHEET 10 OF 27

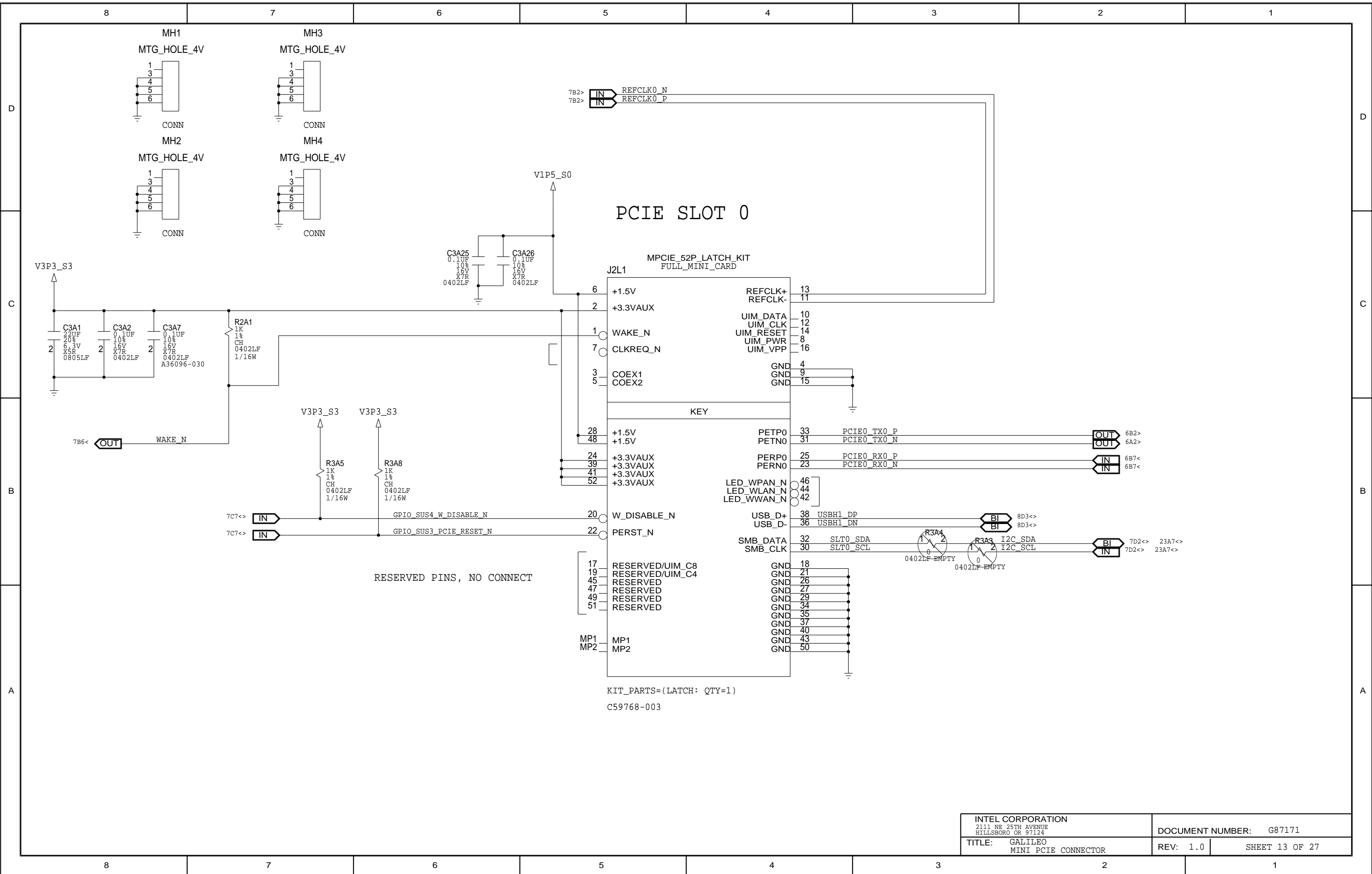


INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO SDRAM 2		REV: 1.0	SHEET 11 OF 27

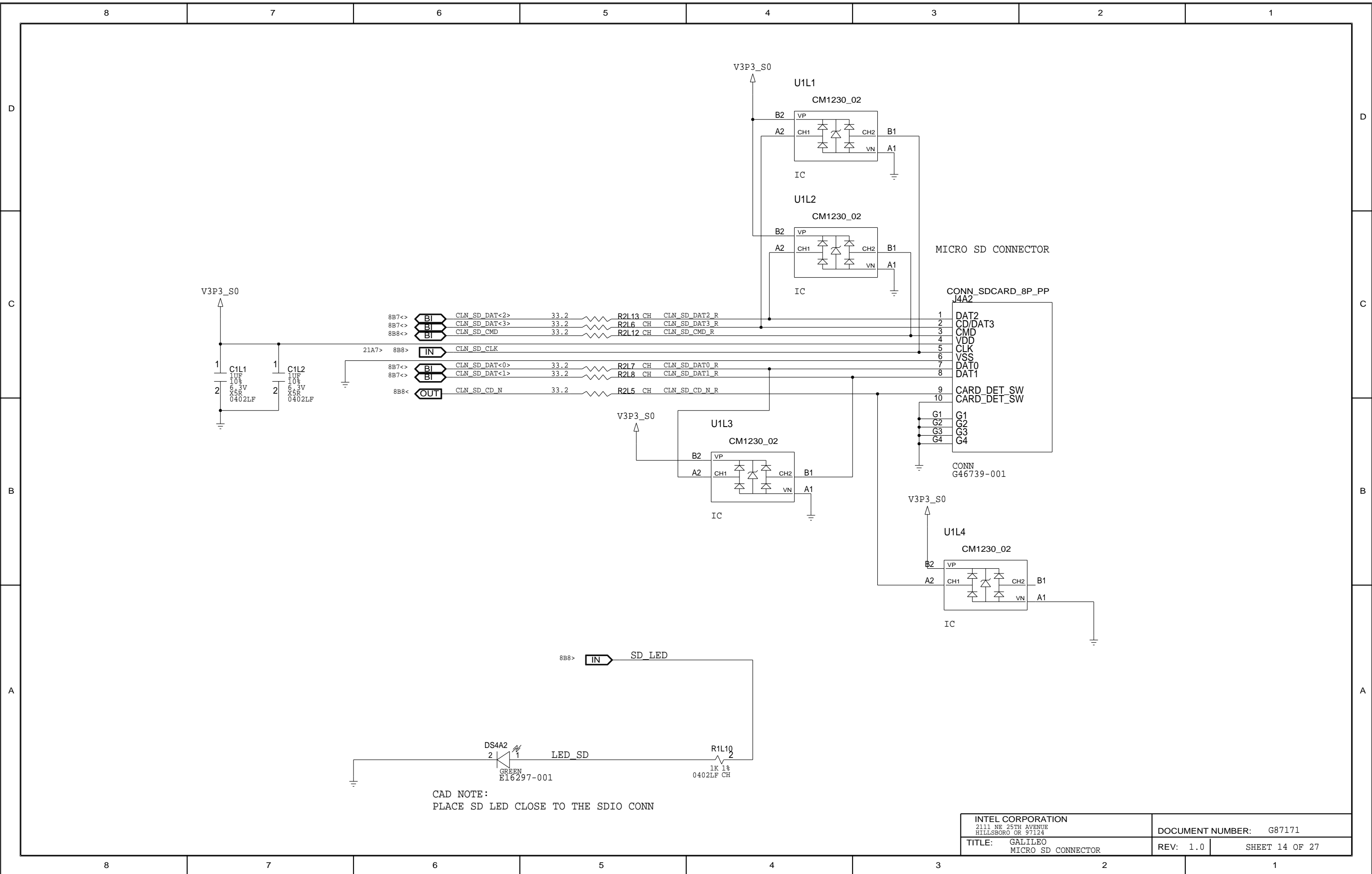


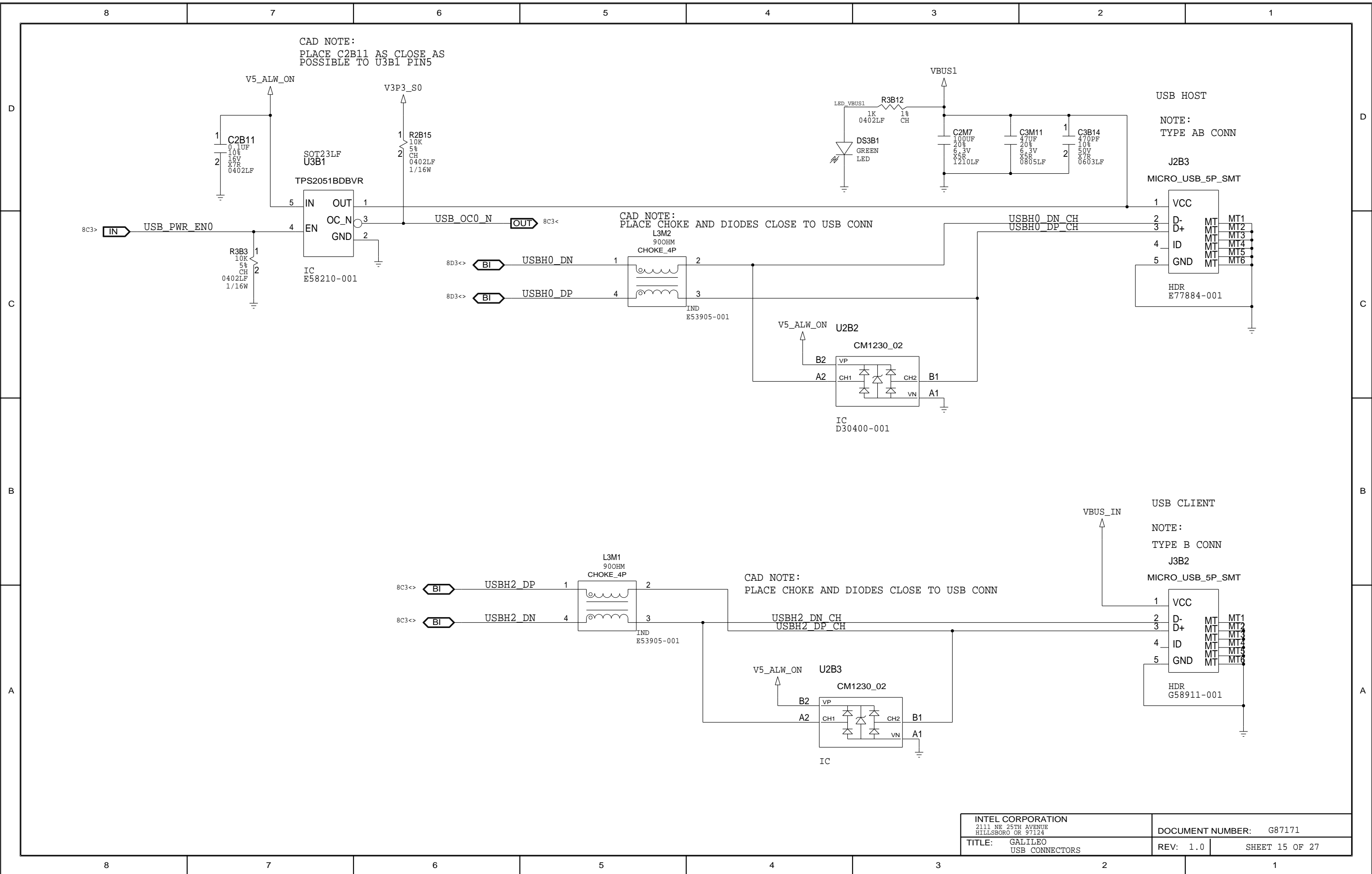
CAD:
DITRIBUTE DECOUPLING AMONG
TERMINATION RESISTORS

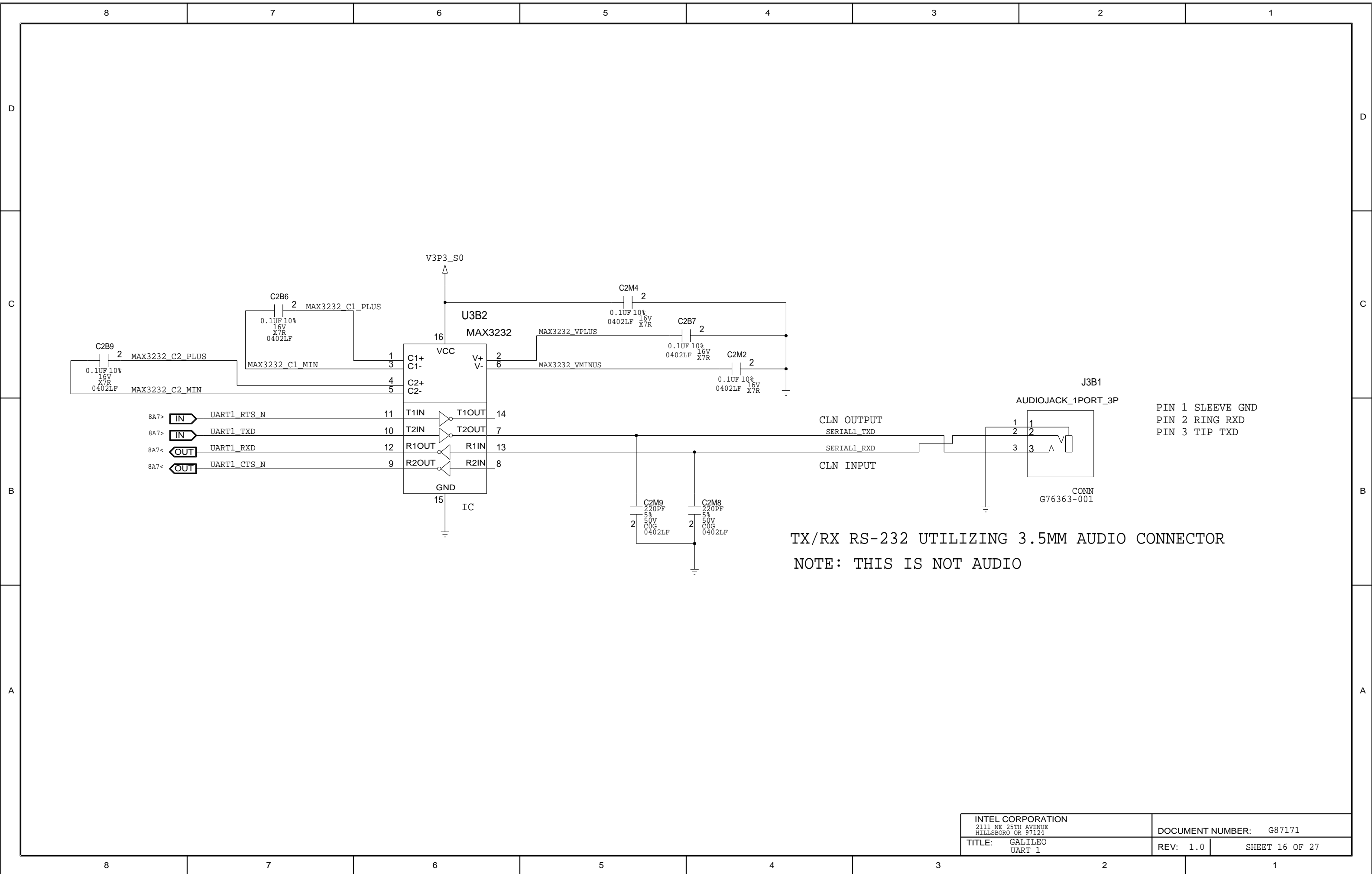
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO SDRAM TERMINATION		REV: 1.0	SHEET 12 OF 27



INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO MINI PCIE CONNECTOR		REV: 1.0	SHEET 13 OF 27

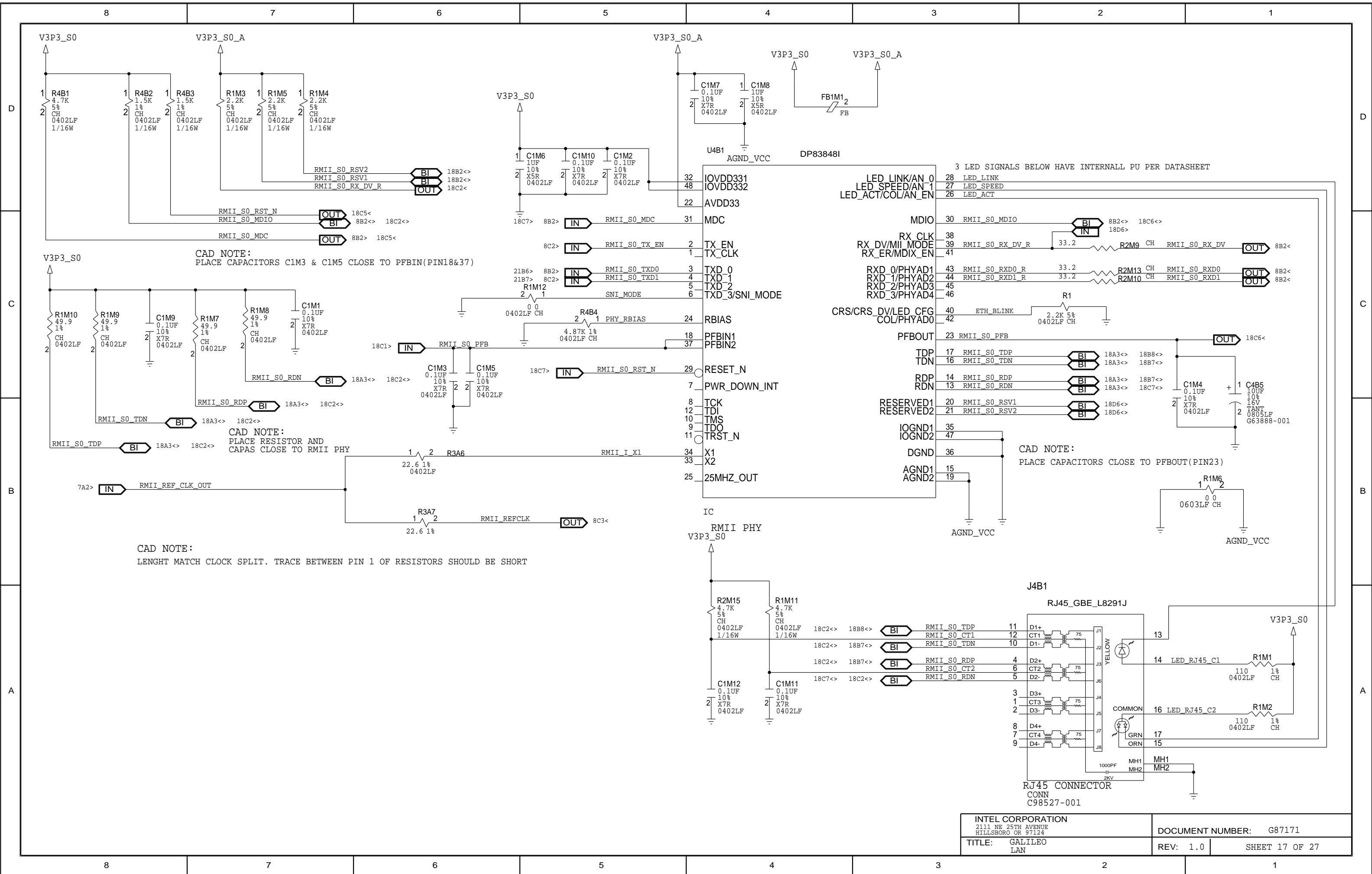




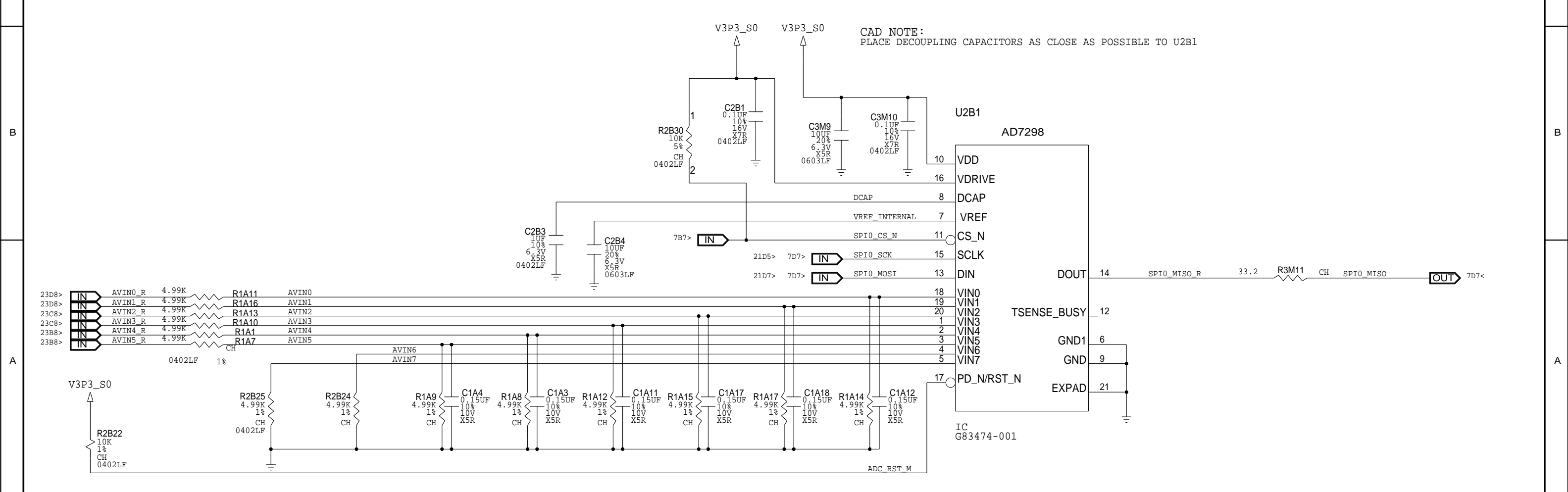
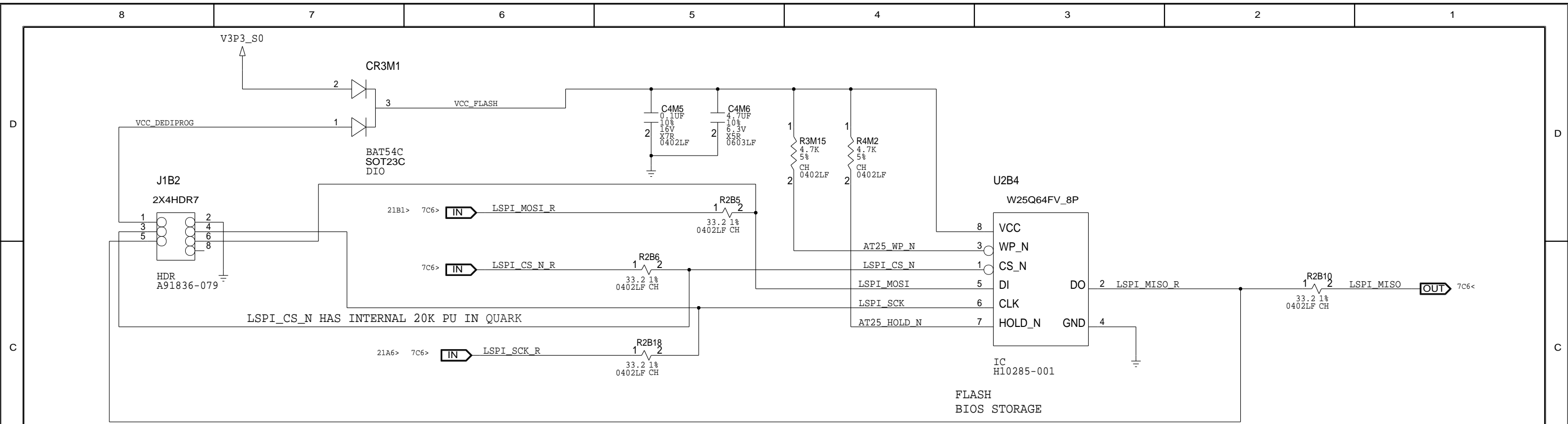


TX/RX RS-232 UTILIZING 3.5MM AUDIO CONNECTOR
 NOTE: THIS IS NOT AUDIO

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO UART 1		REV: 1.0	SHEET 16 OF 27

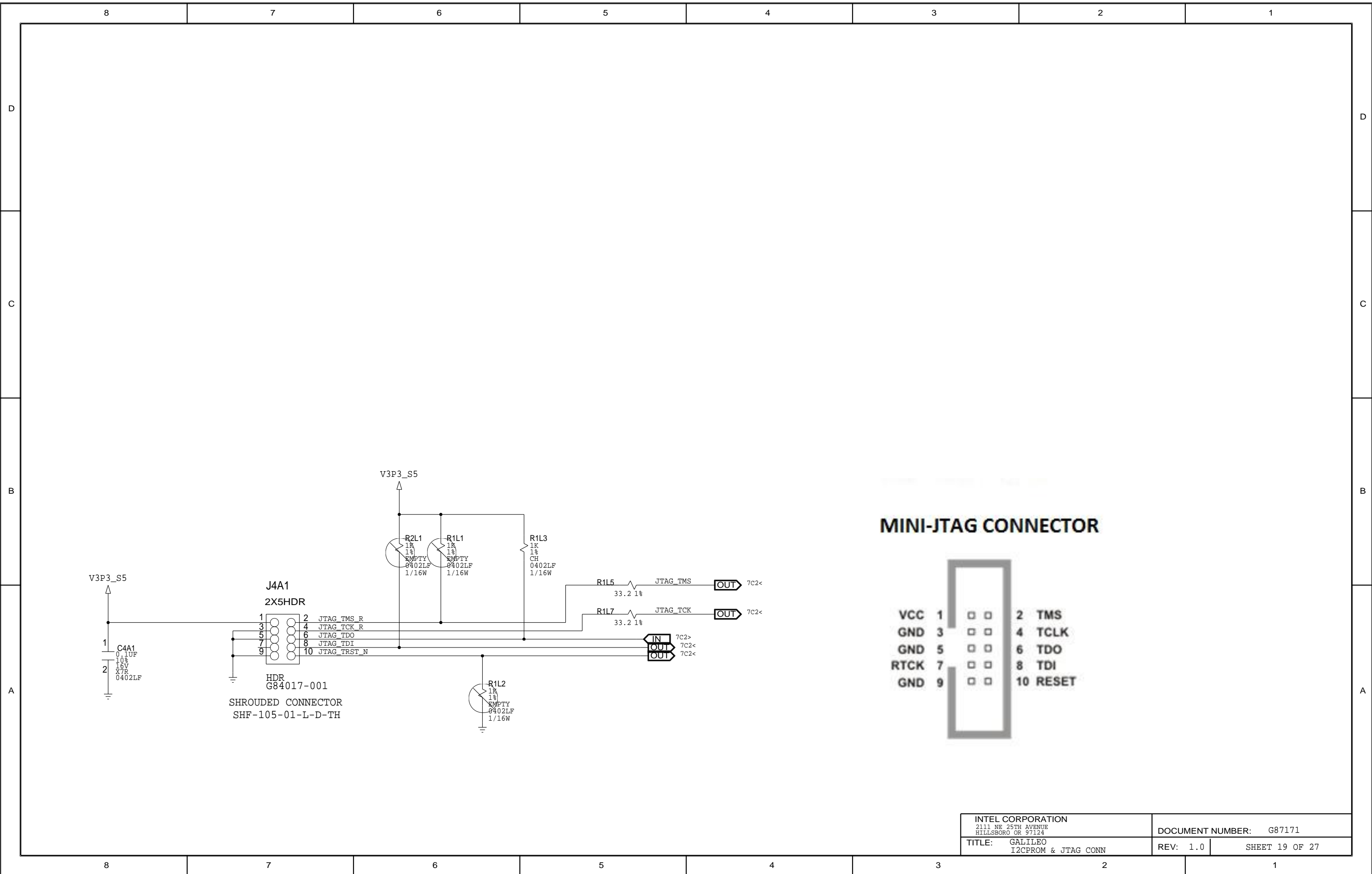


INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171
TITLE: GALILEO LAN	REV: 1.0	SHEET 17 OF 27

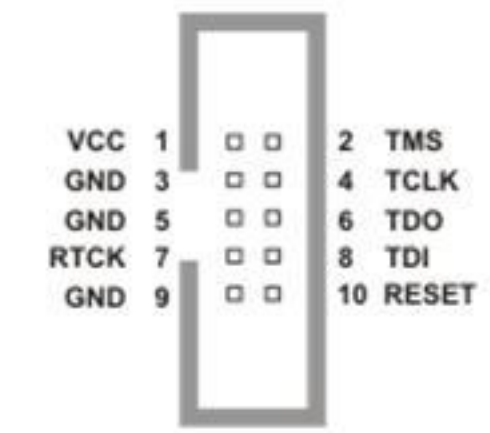


CAD NOTE:
PLACE DECOUPLING CAPACITORS AS CLOSE AS POSSIBLE TO U2B1

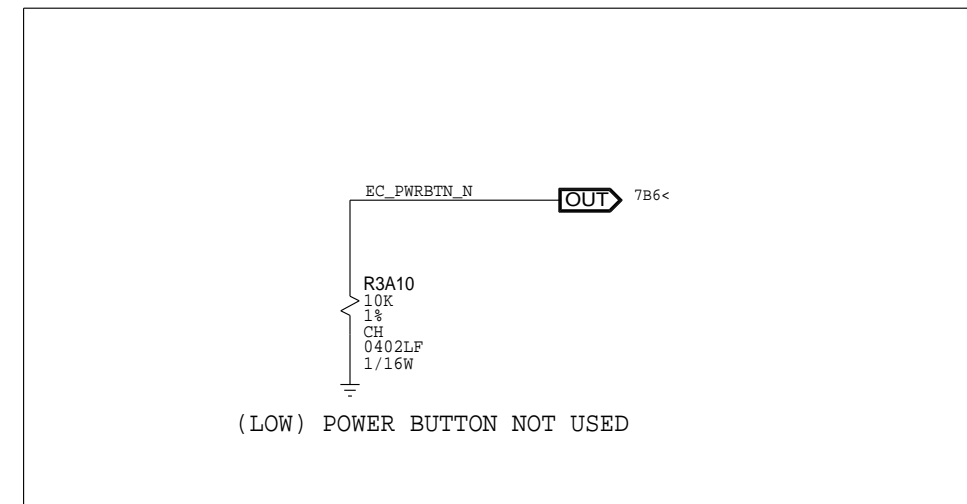
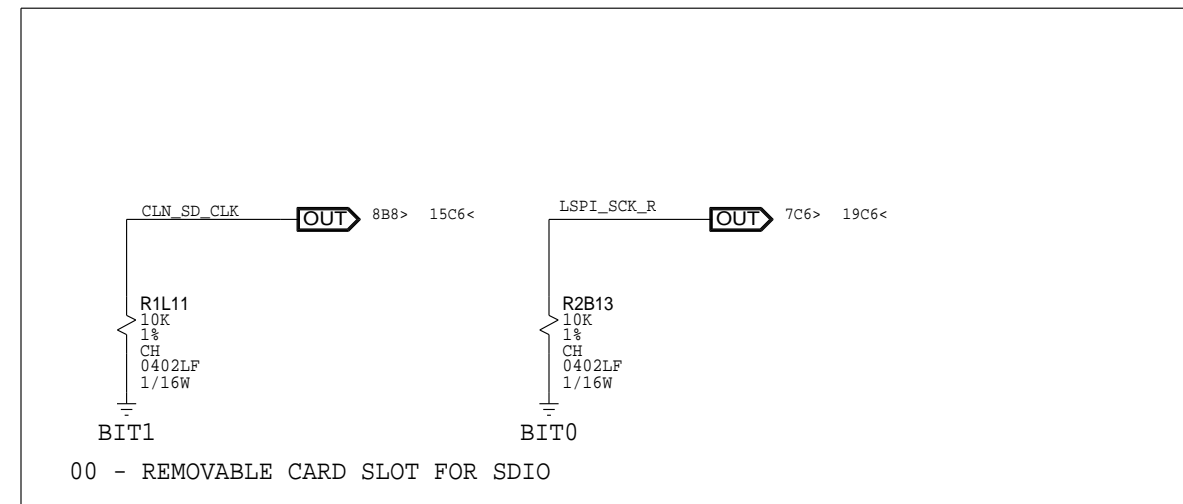
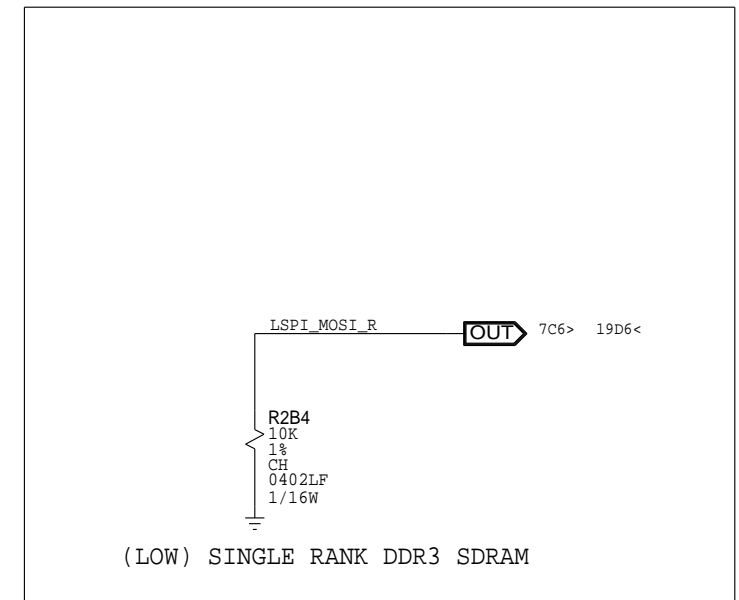
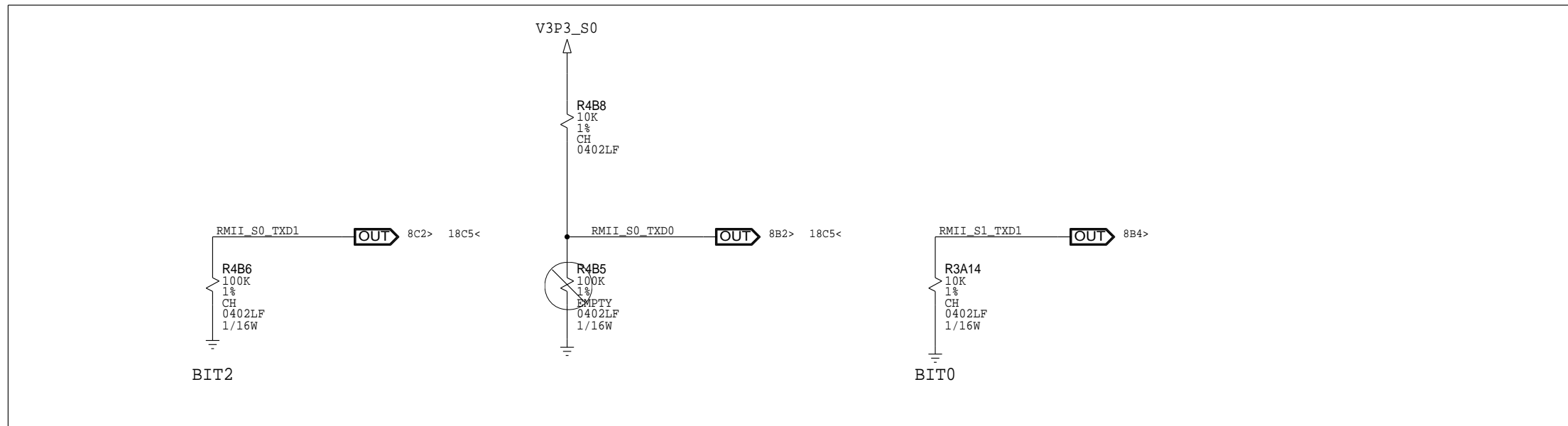
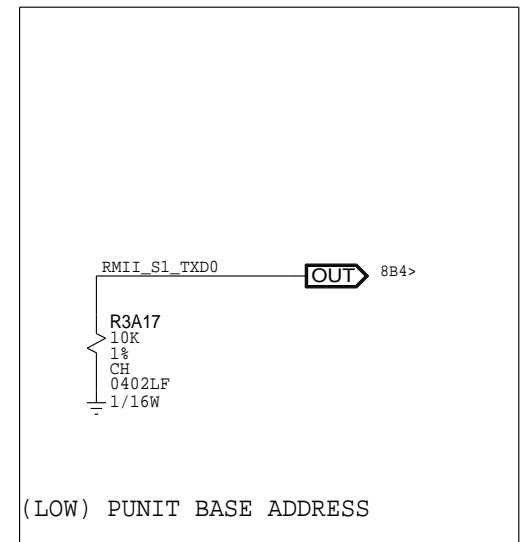
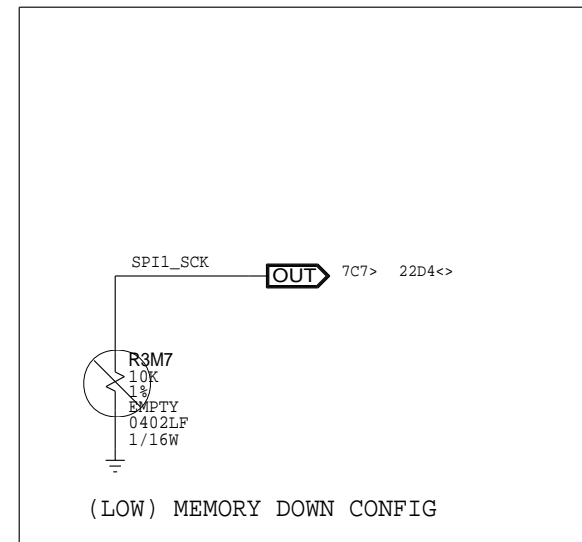
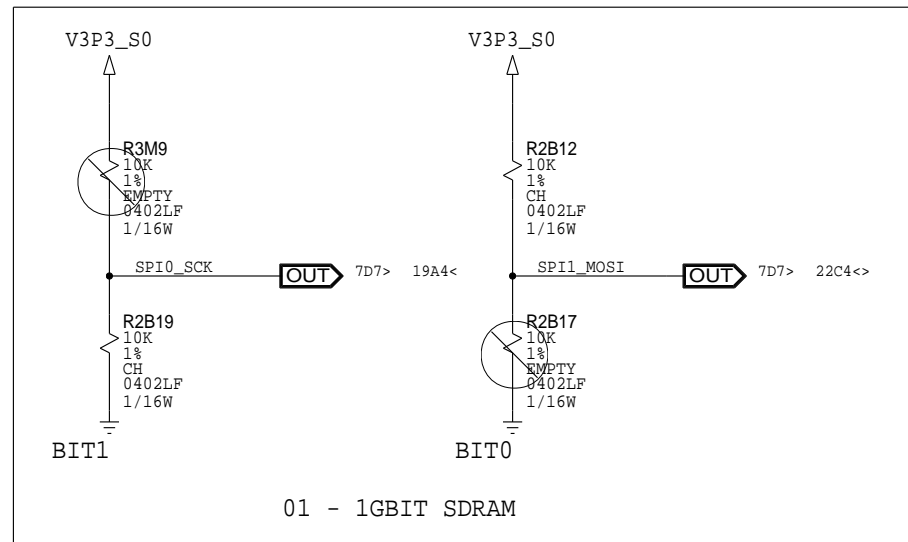
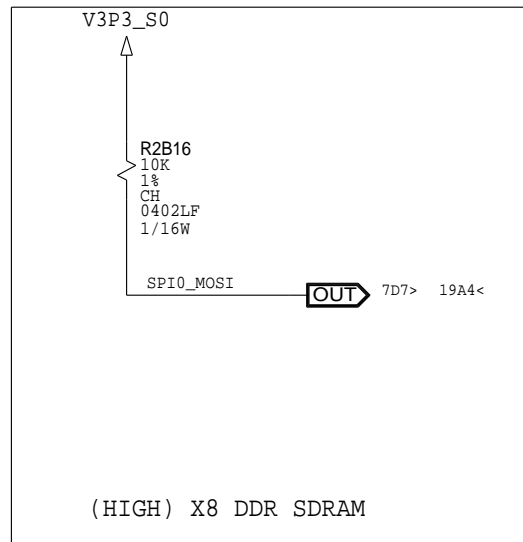
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO SPI: ADC&FLASH		REV: 1.0	SHEET 18 OF 27

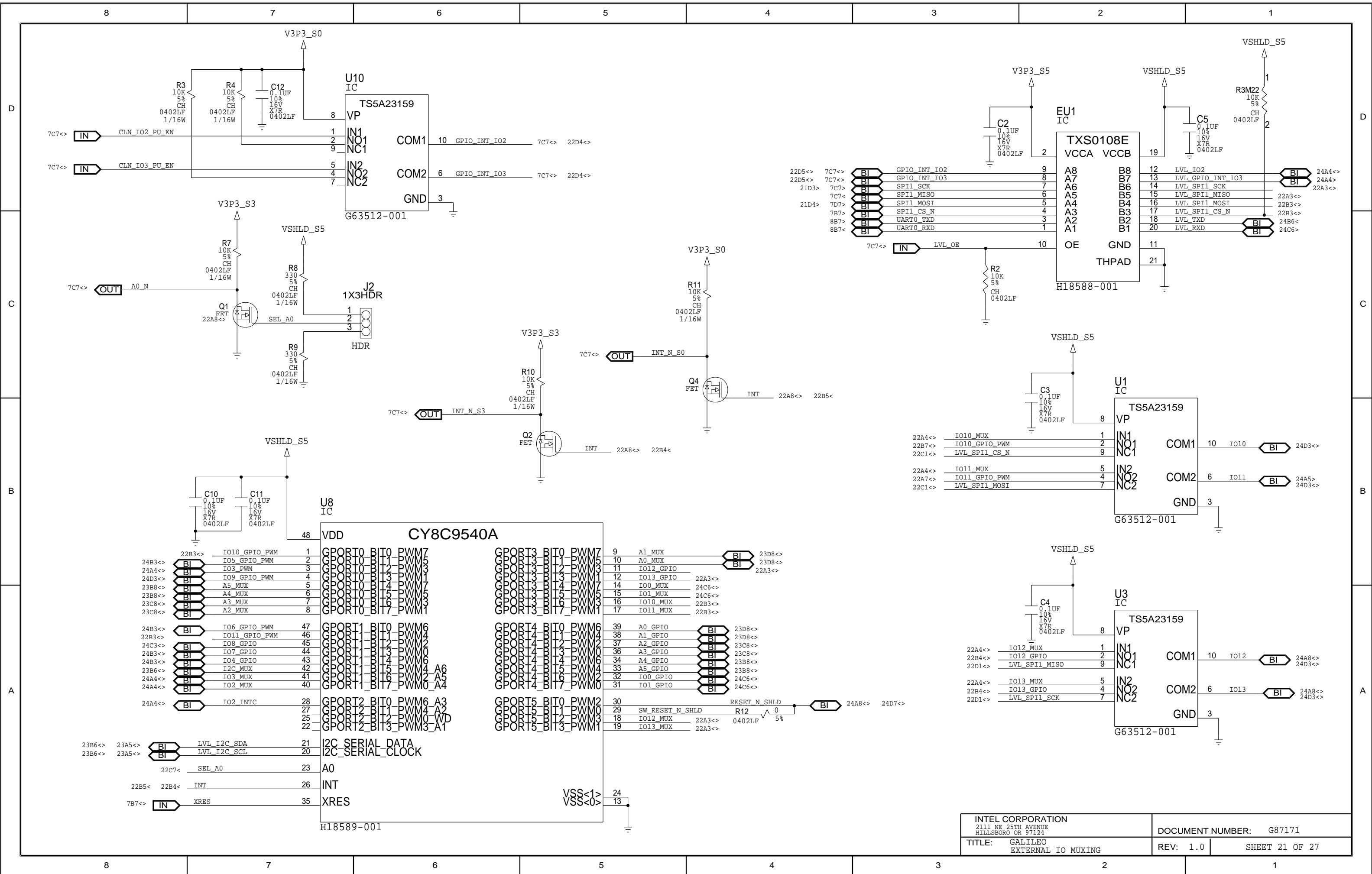


MINI-JTAG CONNECTOR

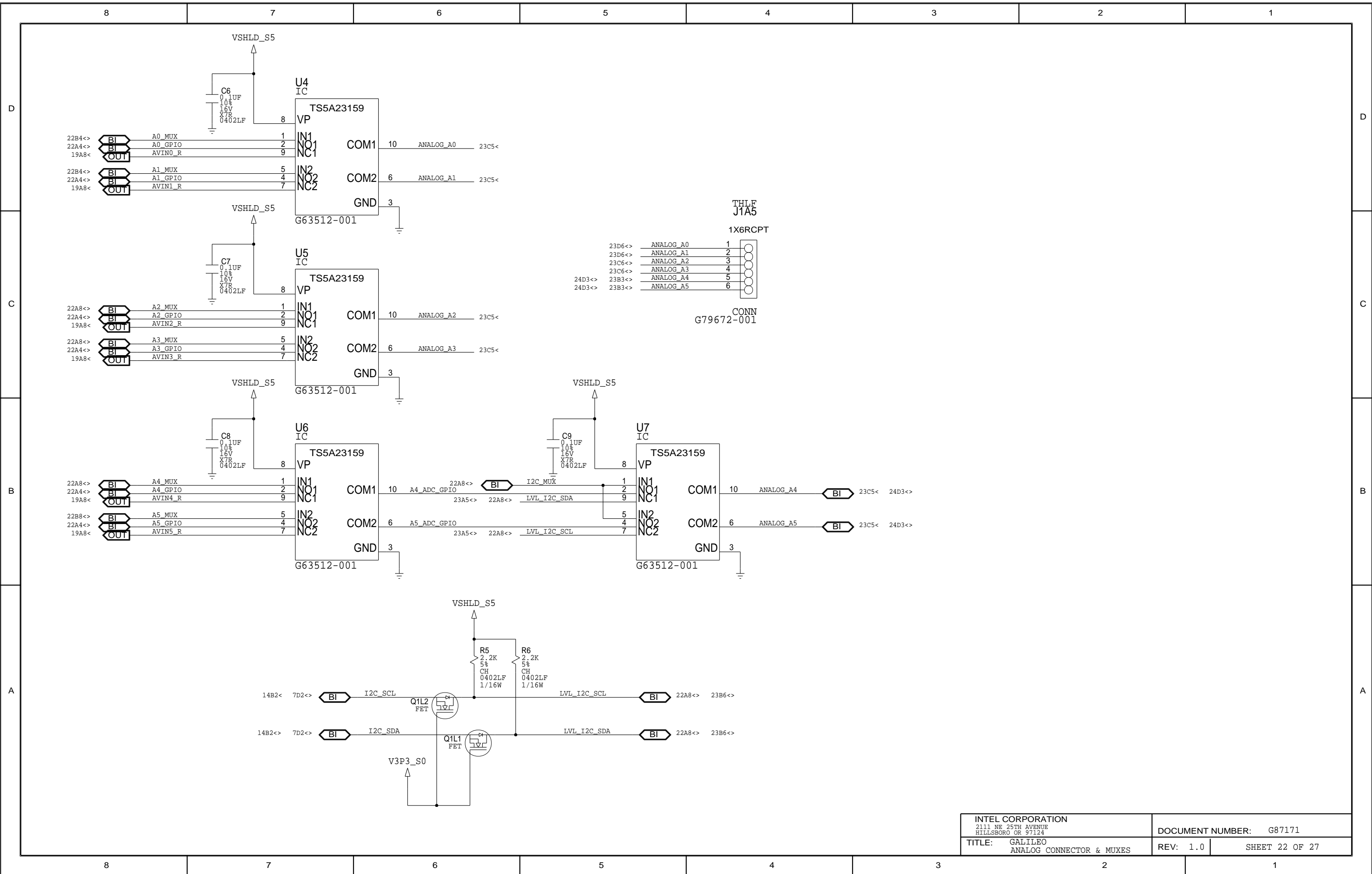


INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO I2CPROM & JTAG CONN		REV: 1.0	SHEET 19 OF 27





INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO EXTERNAL IO MUXING		REV: 1.0	SHEET 21 OF 27

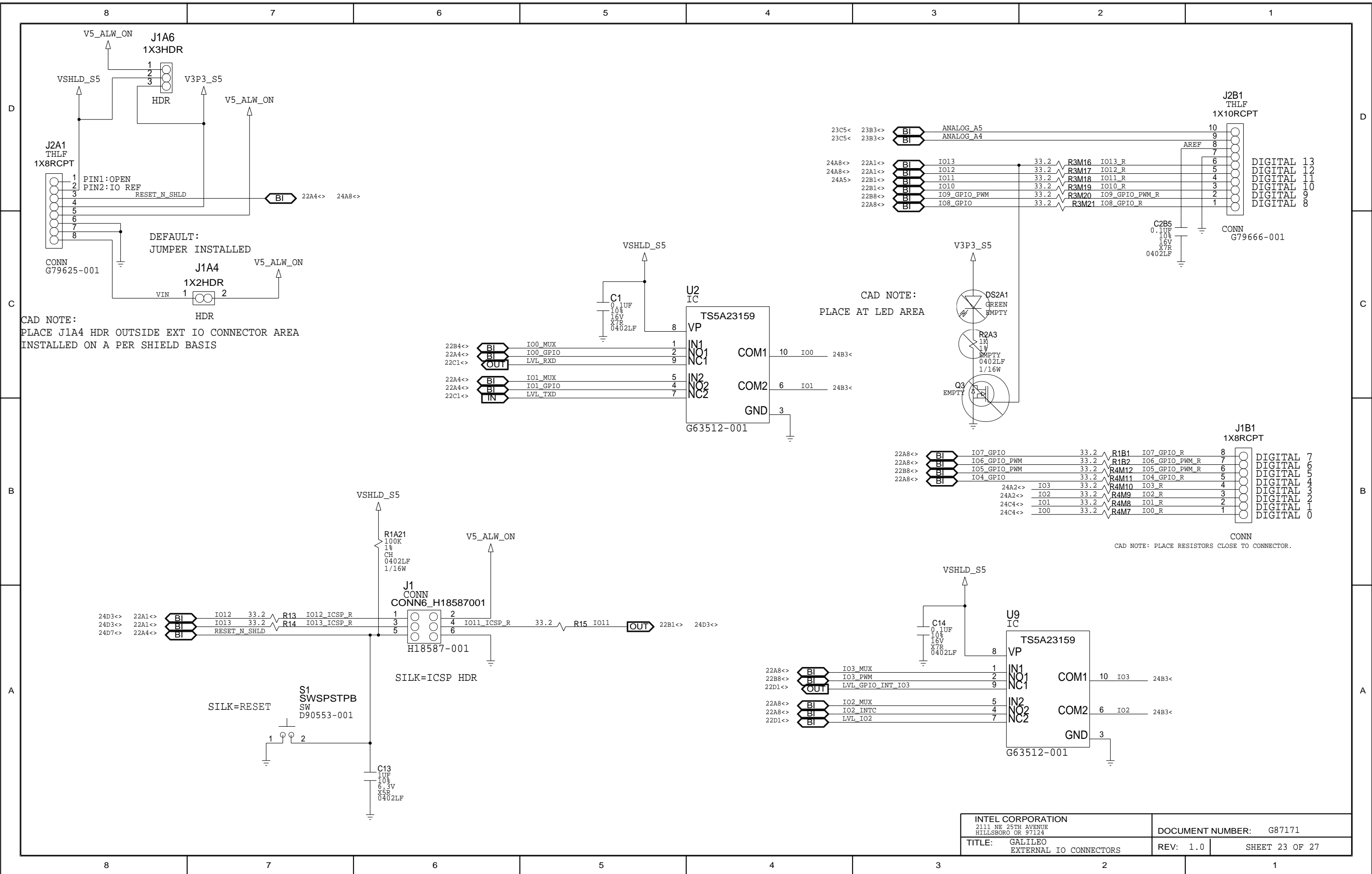


THLF J1A5
1X6RCPT

23D6<>	ANALOG_A0	1	
23D6<>	ANALOG_A1	2	
23C6<>	ANALOG_A2	3	
23C6<>	ANALOG_A3	4	
24D3<>	23B3<>	ANALOG_A4	5
24D3<>	23B3<>	ANALOG_A5	6

CONN G79672-001

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO ANALOG CONNECTOR & MUXES		REV: 1.0	SHEET 22 OF 27

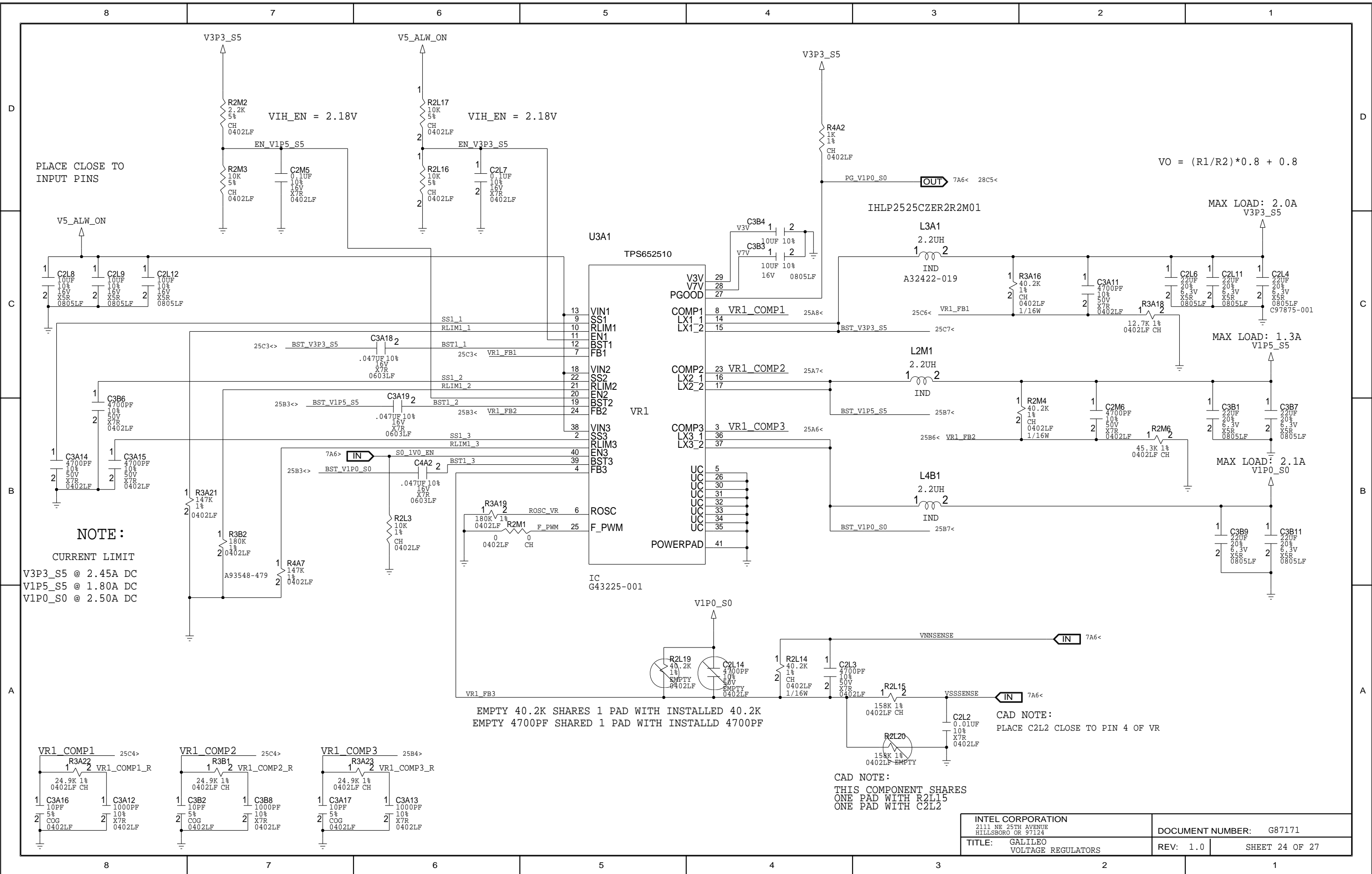


CAD NOTE:
PLACE J1A4 HDR OUTSIDE EXT IO CONNECTOR AREA
INSTALLED ON A PER SHIELD BASIS

CAD NOTE:
PLACE AT LED AREA

CAD NOTE: PLACE RESISTORS CLOSE TO CONNECTOR.

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO EXTERNAL IO CONNECTORS		REV: 1.0	SHEET 23 OF 27



PLACE CLOSE TO INPUT PINS

$$VO = (R1/R2) * 0.8 + 0.8$$

MAX LOAD: 2.0A
V3P3_S5

MAX LOAD: 1.3A
V1P5_S5

MAX LOAD: 2.1A
V1P0_S0

NOTE:

CURRENT LIMIT
 V3P3_S5 @ 2.45A DC
 V1P5_S5 @ 1.80A DC
 V1P0_S0 @ 2.50A DC

EMPTY 40.2K SHARES 1 PAD WITH INSTALLED 40.2K
 EMPTY 4700PF SHARED 1 PAD WITH INSTALLED 4700PF

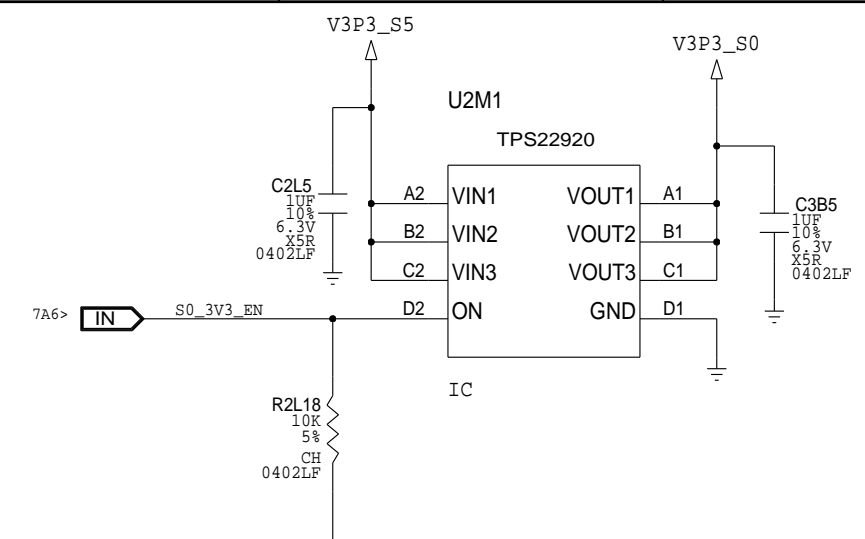
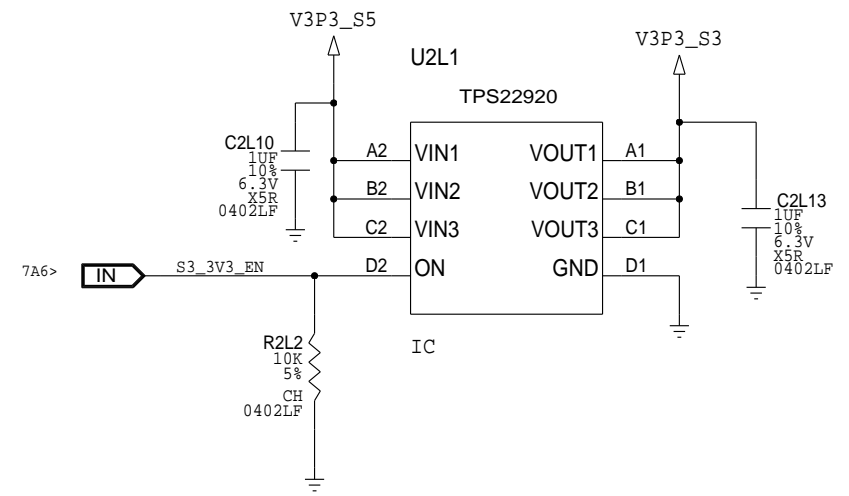
CAD NOTE:
 PLACE C2L2 CLOSE TO PIN 4 OF VR

CAD NOTE:
 THIS COMPONENT SHARES
 ONE PAD WITH R2L15
 ONE PAD WITH C2L2

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO VOLTAGE REGULATORS		REV: 1.0	SHEET 24 OF 27

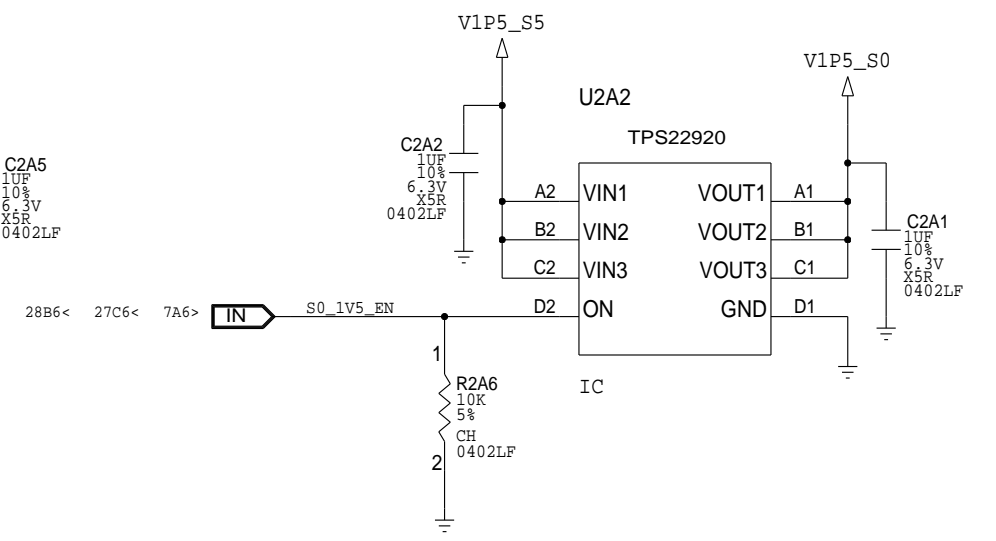
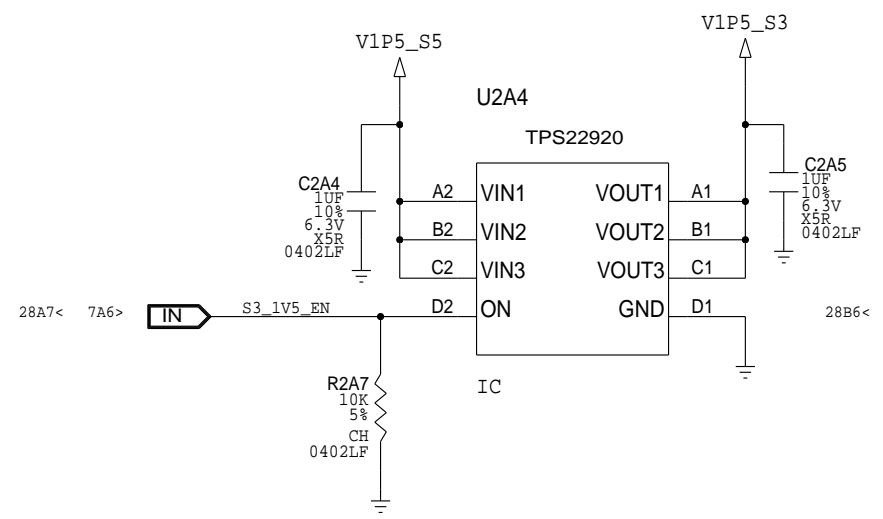
D

V3P3_S5 IS GENERATED W ON-BRD REGULATOR



C

V1P5_S5 IS GENERATED W ON-BRD REGULATOR



CAD NOTE:
PLACE DECOUPLING CAPS AS CLOSE AS POSSIBLE TO SWITCH PINS

B

V1P0_S5 IS GENERATED INTERNALLY

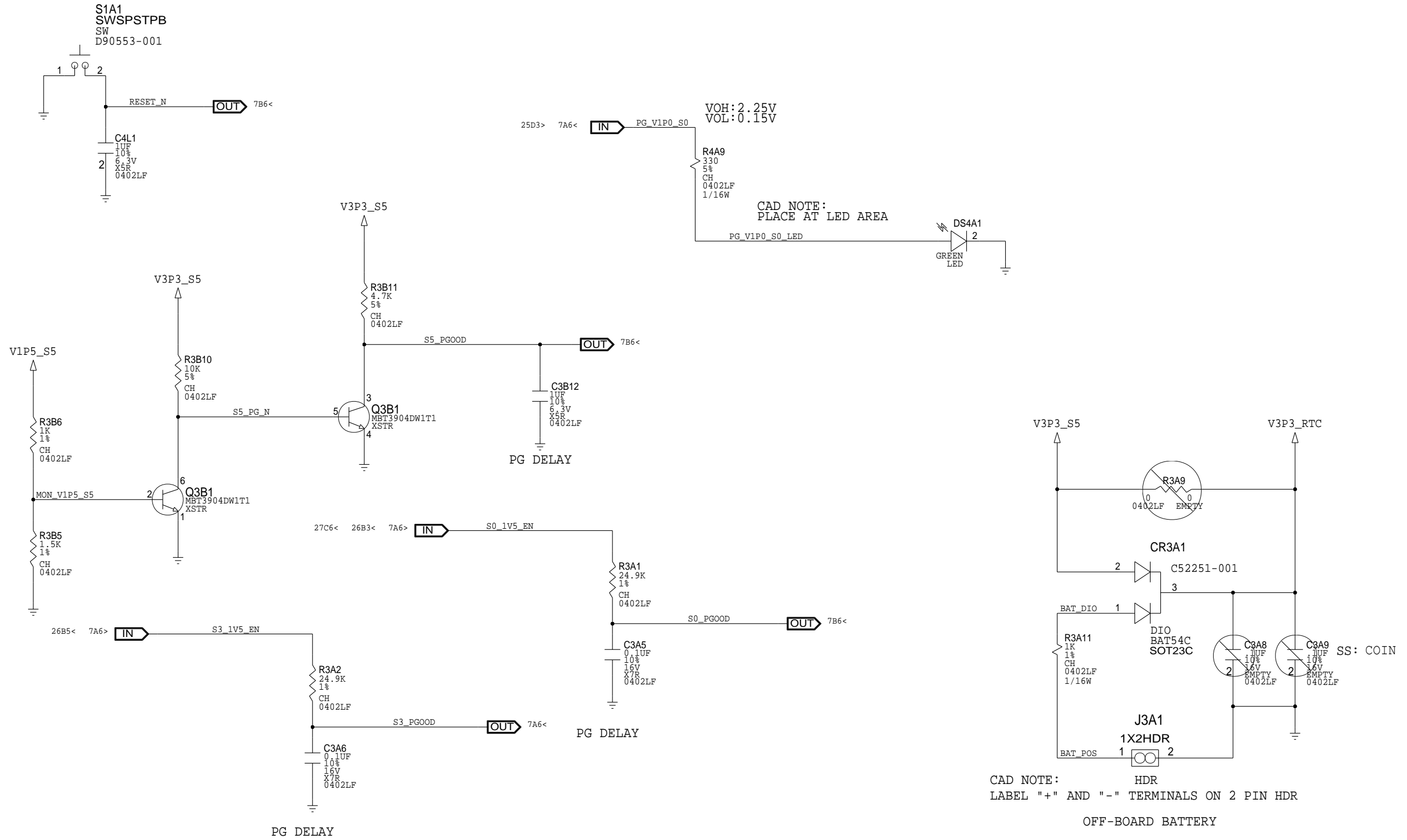
V1P0_S3 IS GENERATED INTERNALLY

V1P0_S0 IS GENERATED W ON-BRD REGULATOR

A

NOTE: RESET_N HAS AN INTERNAL PU TO V3P3_S3

SS:
REBOOT



INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO POWER BUTTONS & MISC		REV: 1.0	SHEET 27 OF 27