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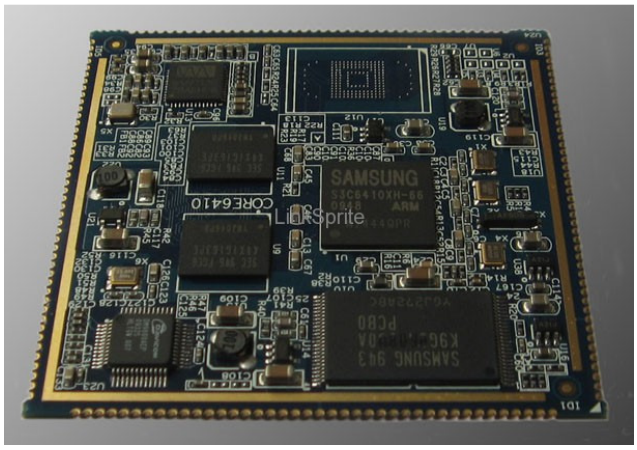
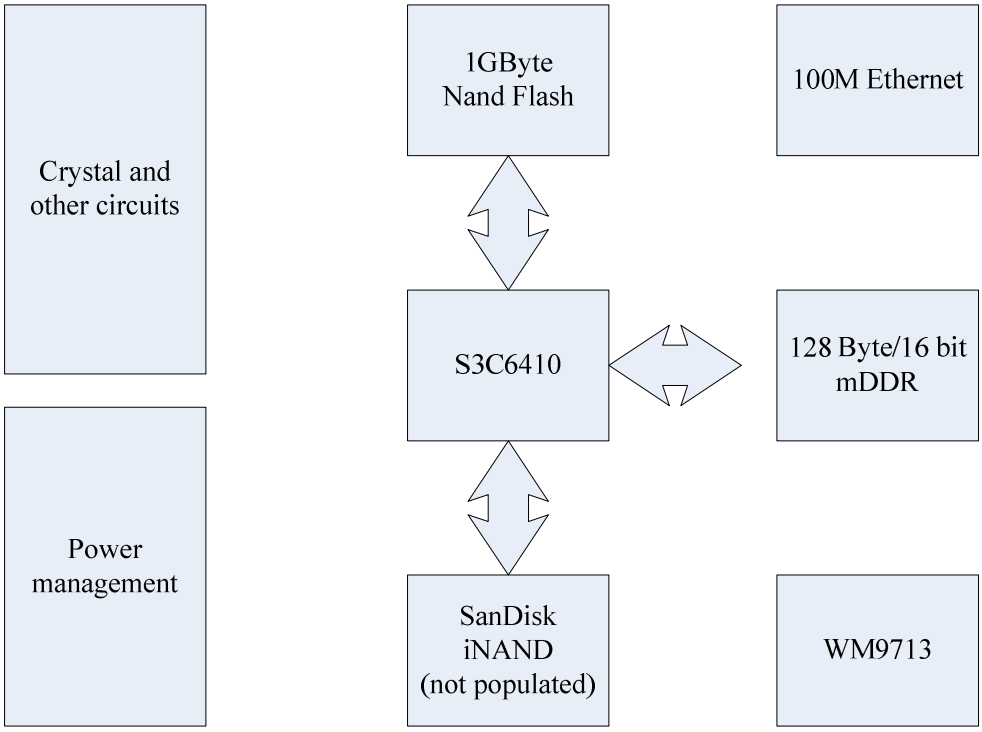
LS6410 S3C6410 ARM11 Core Board



LS6410CORE integrates S3C6410, two 16 bit 128MB mobile DDR, 1GB MLC NAND Flash K9G8G08, power management circuit, Ethernet chip DM9000AEP, audio IC WM9713 of dual input channels/dual output channels, iNand Flash, etc.



1. Pin Definition

Pin	Name	Description	Note	Additional Function
1	KP_COL3	Keypad matrix column scan 3		IO
2	KP_COL4	Keypad Matrix column scan 4		IO
3	KP_COL5	Keypad matrix column scan 5		IO
4	KP_COL6	Keypad matrix column scan 6		IO
5	KP_COL7	Keypad matrix column scan 7		IO
6	EINT20	External interrupt 20		IO
7	EINT21	External interrupt 21		IO
8	PWR_ON_OFF	Power enable, active high		
9	GND	Power ground		
10	CLK_32K	32.768KHz waveform output		
11	SD0_CD	SDIO channel 0 enable, active low	10K resister pull up	IO or EINT12
12	SD0_D0	Data line 0 of SDIO channel 0	10K resister pull up	IO
13	SD0_D1	Data line 1 of SDIO channel 0	10K resister pull up	IO
14	SD0_D2	Data line 2 of SDIO channel 0	10K resister pull up	IO
15	SD0_D3	Data line 3 of SDIO channel 0	10K resister pull up	IO
16	SD0_CLK	Clock of SDIO channel 0	10K resister pull up	IO
17	SD0_CMD	Command signal of SDIO channel 0	10K resister pull up	IO
18	XVD0	Data 0 of LCD signal	B0	IO
19	XVD1	Data 1 of LCD signal	B1	IO
20	XVD2	Data 2 of LCD signal	B2	IO
21	XVD3	Data 3 of LCD signal	B3	IO
22	XVD4	Data 4 of LCD signal	B4	IO
23	XVD5	Data 5 of LCD signal	B5	IO
24	XVD6	Data 6 of LCD signal	B6	IO
25	XVD7	Data 7 of LCD signal	B7	IO
26	XVD8	Data 8 of LCD signal	G0	IO
27	XVD9	Data 9 of LCD signal	G1	IO
28	XVD10	Data 10 of LCD signal	G2	IO
29	XVD11	Data 11 of LCD signal	G3	IO
30	XVD12	Data 12 of LCD signal	G4	IO
31	XVD13	Data 13 of LCD signal	G5	IO
32	XVD14	Data 14 of LCD signal	R6	IO
33	XVD15	Data 15 of LCD signal	R7	IO
34	XVD16	Data 16 of LCD signal	R0	IO

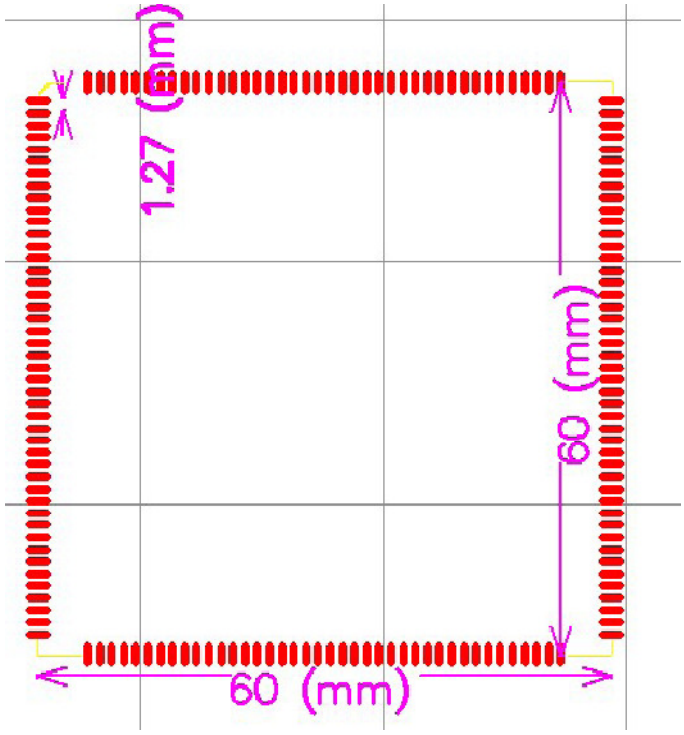
35	XVD17	Data 17 of LCD signal	R1	IO
36	XVD18	Data 18 of LCD signal	R2	IO
37	XVD19	Data 19 of LCD signal	R3	IO
38	XVD20	Data 20 of LCD signal	R4	IO
39	XVD21	Data 21 of LCD signal	R5	IO
40	XVD22	Data 22 of LCD signal	R6	IO
41	XVD23	Data 23 of LCD signal	R7	IO
42	XHSYNC	Raw Scan Signal of LCD		IO
43	XVSYNC	Column Scan Signal of LCD		IO
44	XVDEN	DE signal of LCD		IO
45	XVCLK	Clock signal of LCD		IO
46	CTS1	Serial port 1 TTL CTS		IO
47	RXD1	Serial Port 1 TTL RXD		IO
48	RTS1	Serial Port 1 TTL RTS		IO
49	TXD1	Serial Port 1 TTL TXD		IO
50	GND	Power Gound		IO
51	EINT0	External Interrupt 0		IO
52	EINT1	External Interrupt 1		IO
53	EINT2	External Interrupt 2		IO
54	EINT5	External Interrupt 5		IO
55	EINT6	External Interrupt 6	Can only triggered by high level	IO
56	EINT9	External Interrupt 9		IO
57	EINT10	External Interrupt 10		IO
58	EINT11	External Interrupt 11		IO
59	EINT13	External Interrupt 13	Used to select NAND during booting	IO
60	EINT14	External Interrupt 14	Used to select NAND during booting	IO
61	EINT15	External Interrupt 15	Used to select NAND during booting	IO
62	EINT16	External Interrupt 16		IO
63	EINT17	External Interrupt 17		IO
64	EINT18	External Interrupt 18		IO
65	MIC1	Single channel MIC input		
66	HOST_D-	USB HOST D- pin		
67	HOST_D+	USD HOST D+ pin		
68	PWM1	PWM output 1		IO
69	PWM0	PWM output 0		IO
70	BBP	MIC differential input +	Connect to GSM audio output	
71	BBN	MIC differential input -	Connect to GSM audio output	
72	SPKL	Audio output Left channel		

73	SPKR	Audio output Right channel		
74	MIC_MTN	Audio output -	Connect to GSM audio input	
75	MIC_MTP	Audio output+	Connect to GSM audio input	
76	MICP	MIC input +		
77	MICN	MIC input -		
78	HP_DET	Headphone plug in detection (active low)	Headphone plug in detection	
79	LOUT	Headphone Left channel		
80	ROUT	Headphone Right channel		
81	AC97_W	Audio IC touch function	5 line touch common pin	
82	AC97_Y-	Audio IC touch Y-		
83	AC97_Y+	Audio IC touch Y+		
84	AC97_X-	Audio IC touch X-		
85	AC97_X+	Audio IC touch X+		
86	OM1	Boot configuration pin	Refer to boot configuration	
87	OM2	Boot Configuration pin	Refer to boot configuration	
88	OM3	Boot Configuration pin	Refer to boot configuration	
89	OM4	Boot Configuration pin	Refer to boot configuration	
90	XciYDATA0	Camera interface data line 0		IO
91	XciYDATA1	Camera interface data line 1		IO
92	XciYDATA2	Camera interface data line 2		IO
93	XciYDATA3	Camera Interface data line 3		IO
94	XciYDATA4	Camera Interface data line 4		IO
95	XciYDATA5	Camera Interface data line 5		IO
96	XciYDATA6	Camera Interface data line 6		IO
97	XciYDATA7	Camera Interface data line 7		IO
98	XciCLK	Camera Interface Clock		IO
99	XciHREF	Horizontal Sync Clock		IO
100	XciPCLK	Pixel Clock Signal		IO
101	XciRSTN	Camera module Reset signal		IO
102	XciVSYNC	Frame Sync Clock Signal		IO
103	RXD0	Serial port 0 TTL RXD		IO
104	TXD0	Serial port 0 TTL TXD		IO
105	CTS0	Serial port 0 TTL CTS		IO
106	RTS0	Serial port 0 TTL RTS		IO
107	RXD2	Serial port 2 TTL RXD		IO
108	TXD2	Serial port 2 TTL TXD		IO
109	RXD3	Serial port 3 TTL RXD		IO
110	TXD3	Serial port 3 TTL TXD		IO
111	XirSDBW	Infra-red control signal		IO
112	GND	Power Ground		

113	NET_SPEED	Network speed indicator output	Active Low	
114	NET_LINK	Network Link indicator output	Active Low	
115	AVDD25	2.5V output	To supply the Ethernet transformer	
116	NET_TX-	Ethernet Differential TX-		
117	NET_TX+	Ethernet Differential TX+		
118	NET_RX-	Ethernet Differential RX-		
119	NET_RX+	Ethernet Differential RX+		
120	SPI0_MISO	SPI channel 0 MISO		IO or EINT
121	SPI0_CLK	SPI channel 0 CLK		IO or EINT
122	SPI0_MOSI	SPI channel 0 MOSI		IO or EINT
123	SPI0_CS	SPI channel 0 CS		IO or EINT
124	SPI1_MISO	SPI channel 1 MISO	Dual Function: SD2_CMD	IO or EINT
125	SPI1_CLK	SPI channel 1 CLK	Dual Function: SD2_CLK	IO or EINT
126	SPI1_MOSI	SPI channel 1 MOSI		IO or EINT
127	SPI1_CS	SPI channel 1 CS		IO or EINT
128	SD1_CD	SD channel 1 channel selection (active low)		IO
129	SD1_CLK	SD channel 1 CLK		IO
130	SD1_CMD	SD channel 1 Command signal		IO
131	SD1_D0	SD channel 1 data 0		IO
132	SD1_D1	SD channel 1 data 1		IO
133	SD1_D2	SD channel 1 data 2		IO
134	SD1_D3	SD channel 1 data 3		IO
135	SD1_D4	SD channel 1 data 4	Dual function: SD2_D0	IO
136	SD1_D5	SD channel 1 data 5	Dual function: SD2_D1	IO
137	DS1_D6	SD channel 1 data 6	Dual function: SD2_D2	IO
138	SD1_D7	SD channel 1 data 7	Dual function: SD2_D3	IO
139	AIN0	ADC channel 0	ADC precision: 10 bit	
140	AIN1	ADC channel 1		
141	AIN2	ADC channel 2		
142	AIN3	ADC channel 3		
143	TS_YM	Touch Y-		
144	TS_YP	Touch Y+		
145	TS_XM	Touch X-		
146	TS_XP	Touch X+		
147	IIC0_SCL	IIC bus clock	Need external 10K pull up	

148	IIC0_SDA	IIC bus data	Need external 10K pull up	
149	DAC0	TV analog output signal 0	Connect to TV output	
150	DAC1	TV analog output signal 1	Connect to TV output	
151	GND	Power Ground		
152	OTG_D-	OTG Data -		
153	OTG_D+	OTG Data+		
154	OTG_ID	OTG ID signal		
155	OTGDRV_VBUS	OTG power output enable signal		
156	DVBUS	OTG power input detection signal		
157	nRESET	Reset signal (active low)		
158	VDD_RTC	RTC backup battery input	1.8-3.0V	
159	VDD_MAX	Signal main power input	2.7-6.5V	
160	KP_ROW0	Keypad matrix row scan 0		IO
161	KP_ROW1	Keypad matrix row scan 1		IO
162	KP_ROW2	Keypad matrix row scan 2		IO
163	KP_ROW3	Keypad matrix row scan 3		IO
164	KP_ROW4	Keypad matrix row scan 4		IO
165	KP_ROW5	Keypad matrix row scan 5		IO
166	KP_ROW6	Keypad matrix row scan 6		IO
167	KP_ROW7	Keypad matrix row scan 7		IO
168	KP_COL0	Keypad matrix column scan 0		IO
169	KP_COL1	Keypad matrix column scan 1		IO
170	KP_COL2	Keypad matrix column scan 2		IO

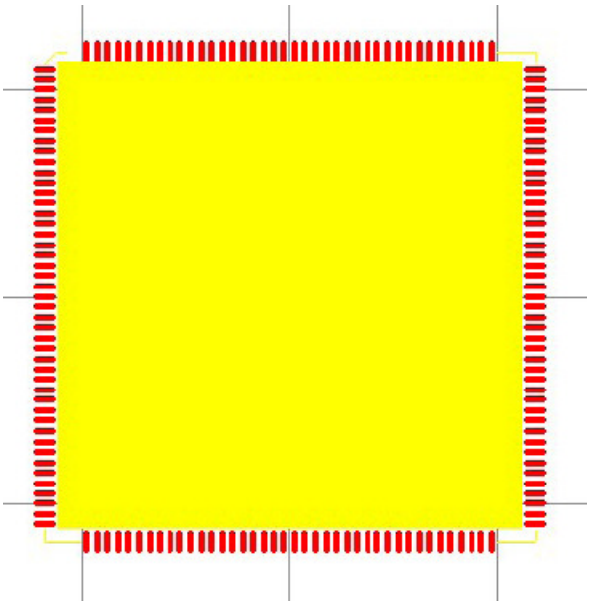
2. Core Board Package



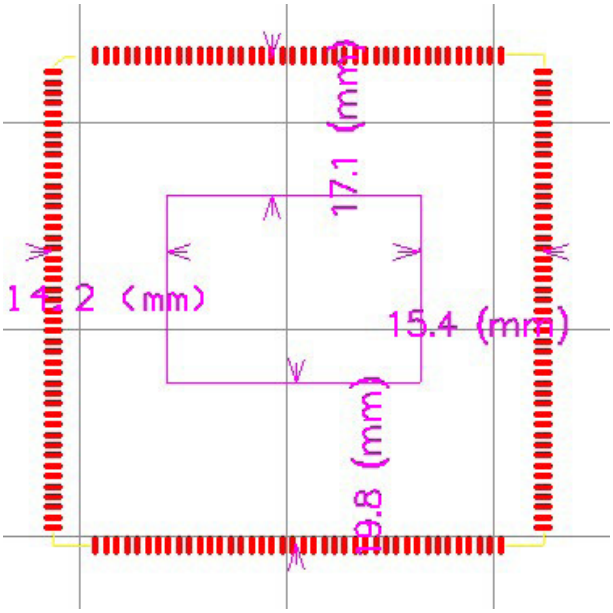
Thickness: 2.85mm
Length: 60mm
Width: 60mm
Pin pitch: 1.27mm

Recommended footprint as follows:

1. Add a layer of silkscreen to prevent the core board shots with via on the motherboard.



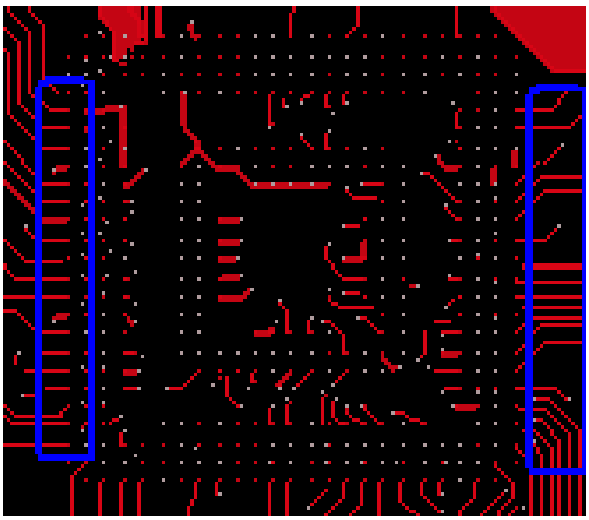
2. Add a rectangle opening on the motherboard as shown in the following figure.



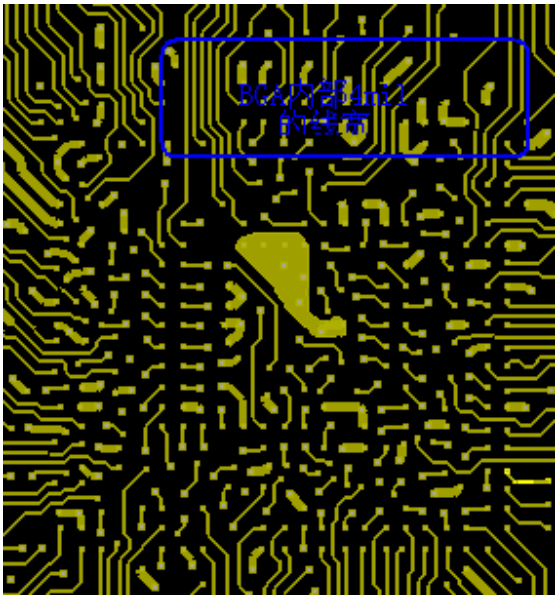
3. PCB Layout

3.1 Core Board PCB normal line width and line interval

1. Normal signal line interval 4 mil.
2. TOP layer: the first line outside BGA has a line interval of 5 mil.



3. Lines under BGA has an interval of 4 mil.

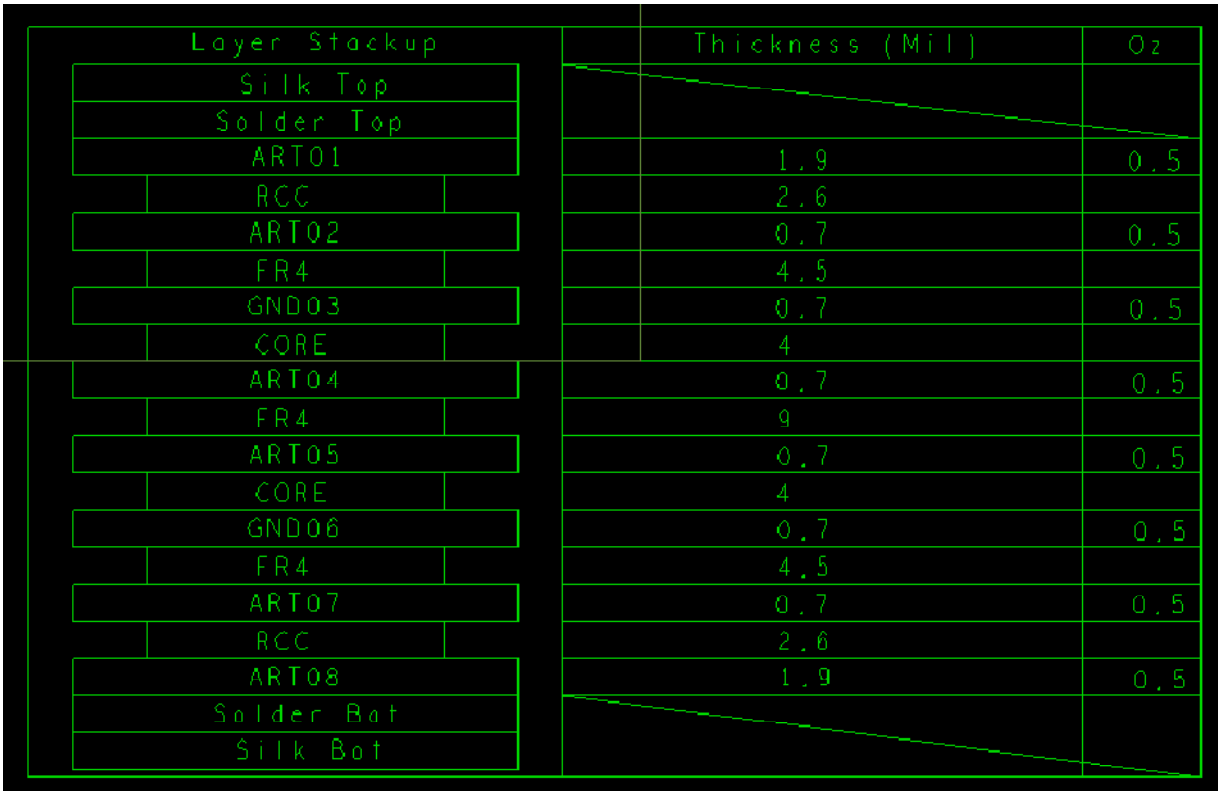


4. The minimal line width of power and GND is 10 mil, and maxium 20 mil.

3.2 Size of via and distribution of blind and buried via

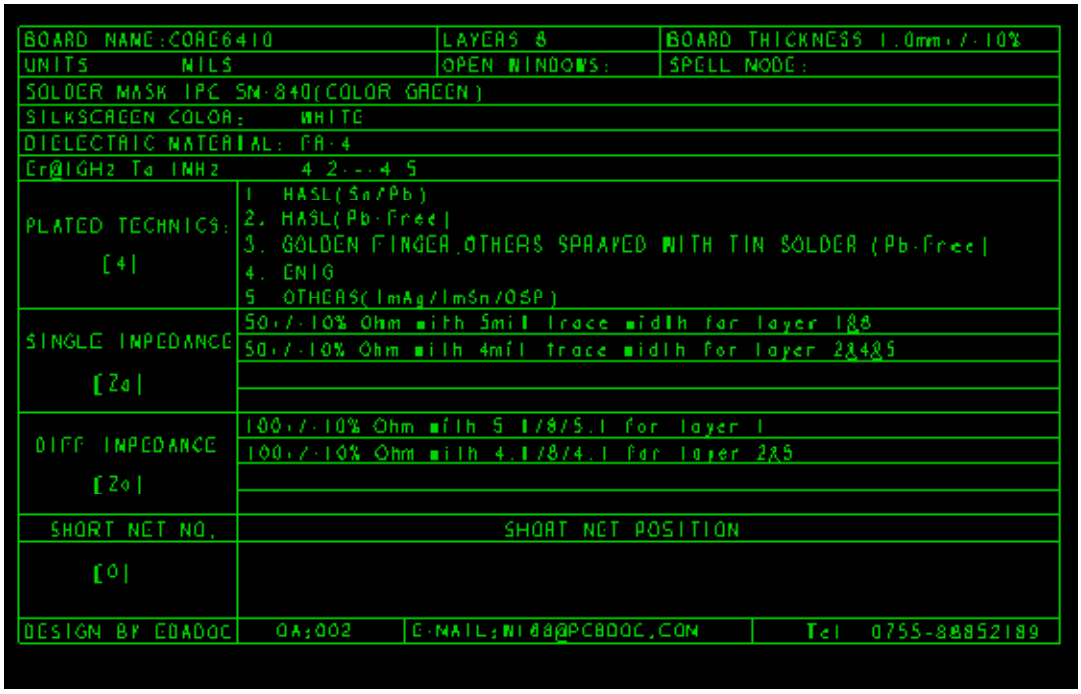
This core board uses blind and buried via. There are no empty via.

3.3 Core Board Stackup



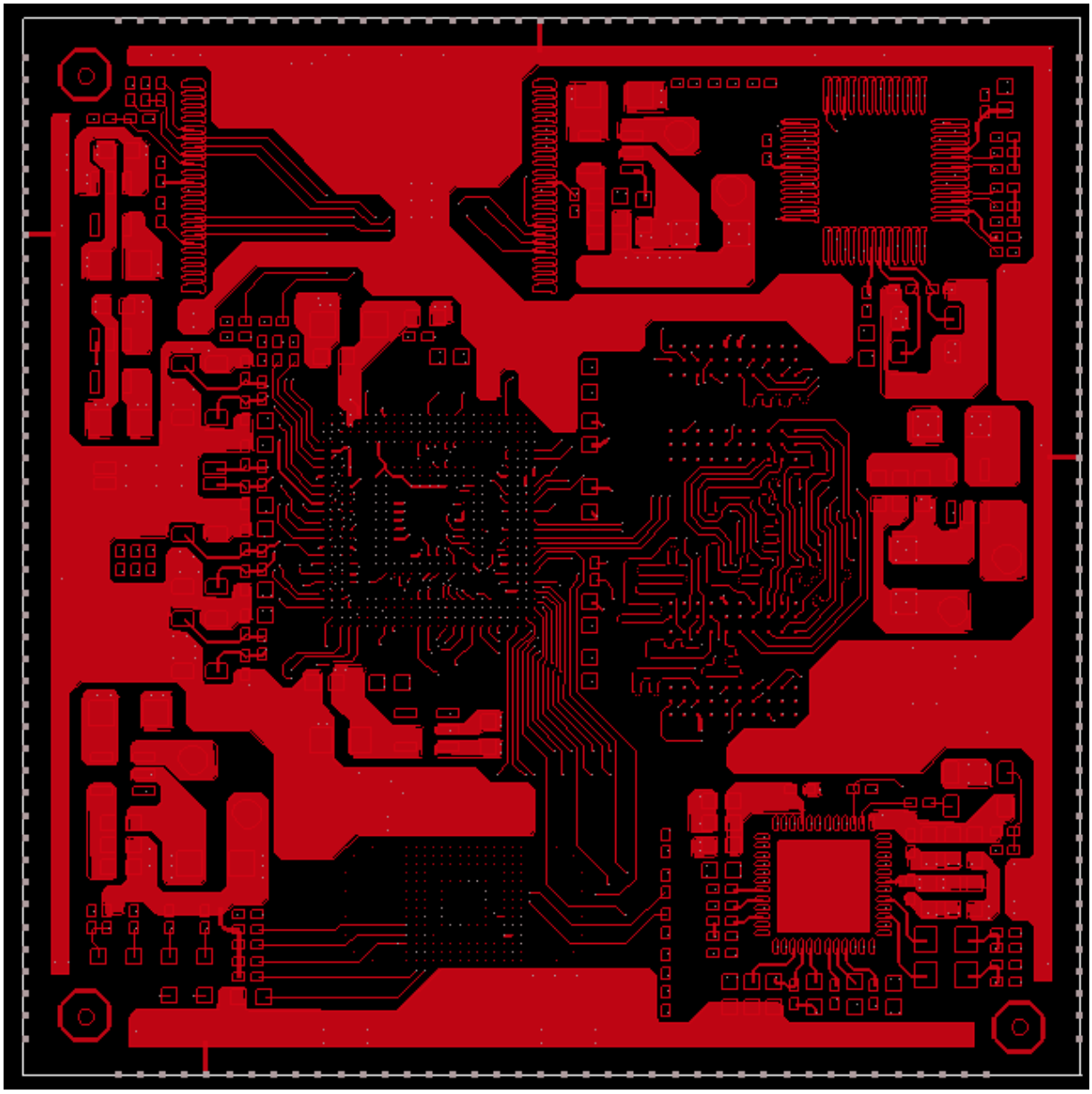
Layer Stackup	Thickness (Mil)	O2
Silk Top		
Solder Top		
ART01	1.9	0.5
RCC	2.6	
ART02	0.7	0.5
FR4	4.5	
GND03	0.7	0.5
CORE	4	
ART04	0.7	0.5
FR4	9	
ART05	0.7	0.5
CORE	4	
GND06	0.7	0.5
FR4	4.5	
ART07	0.7	0.5
RCC	2.6	
ART08	1.9	0.5
Solder Bot		
Silk Bot		

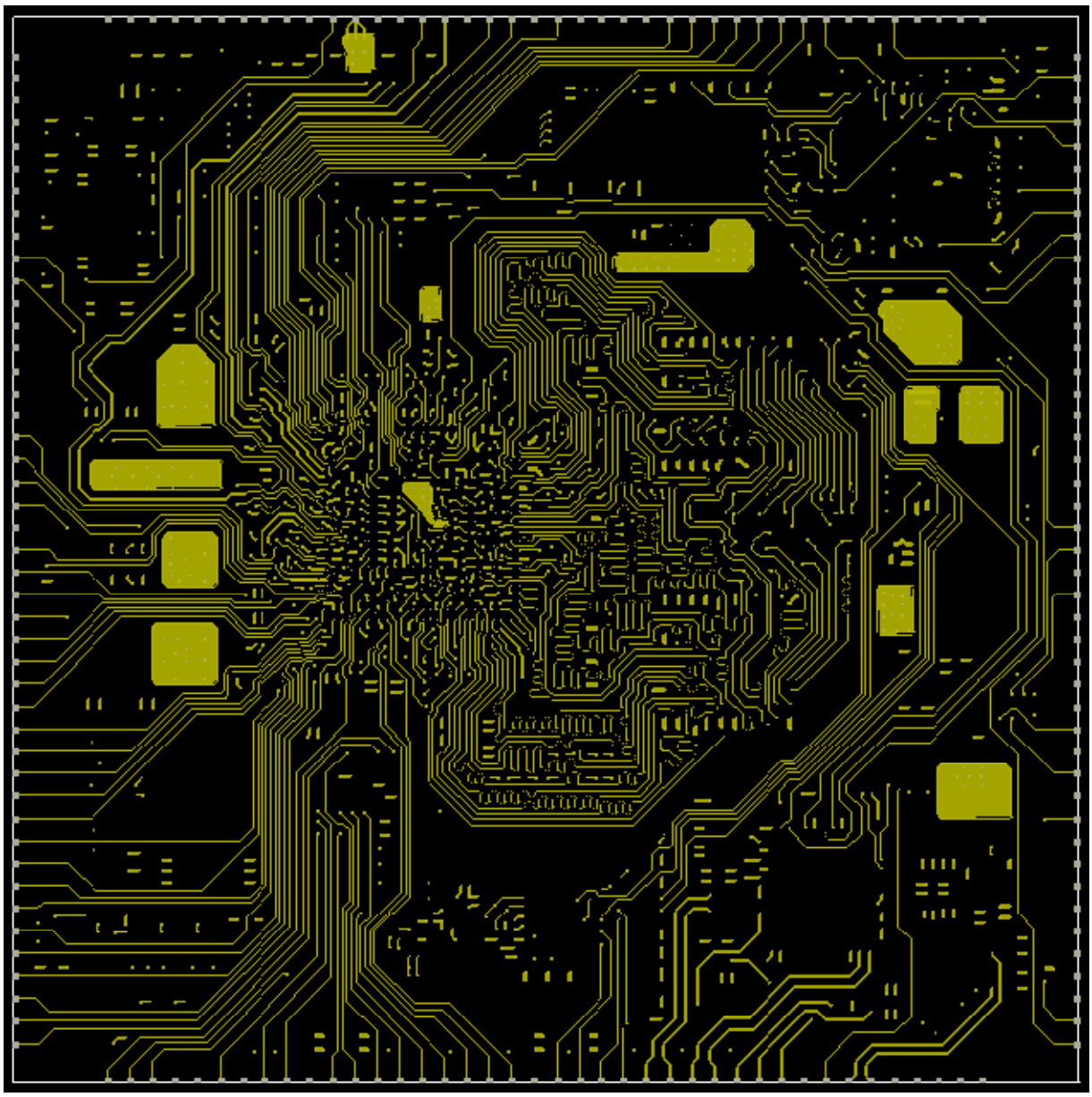
3.4 Core Board Impedance Control

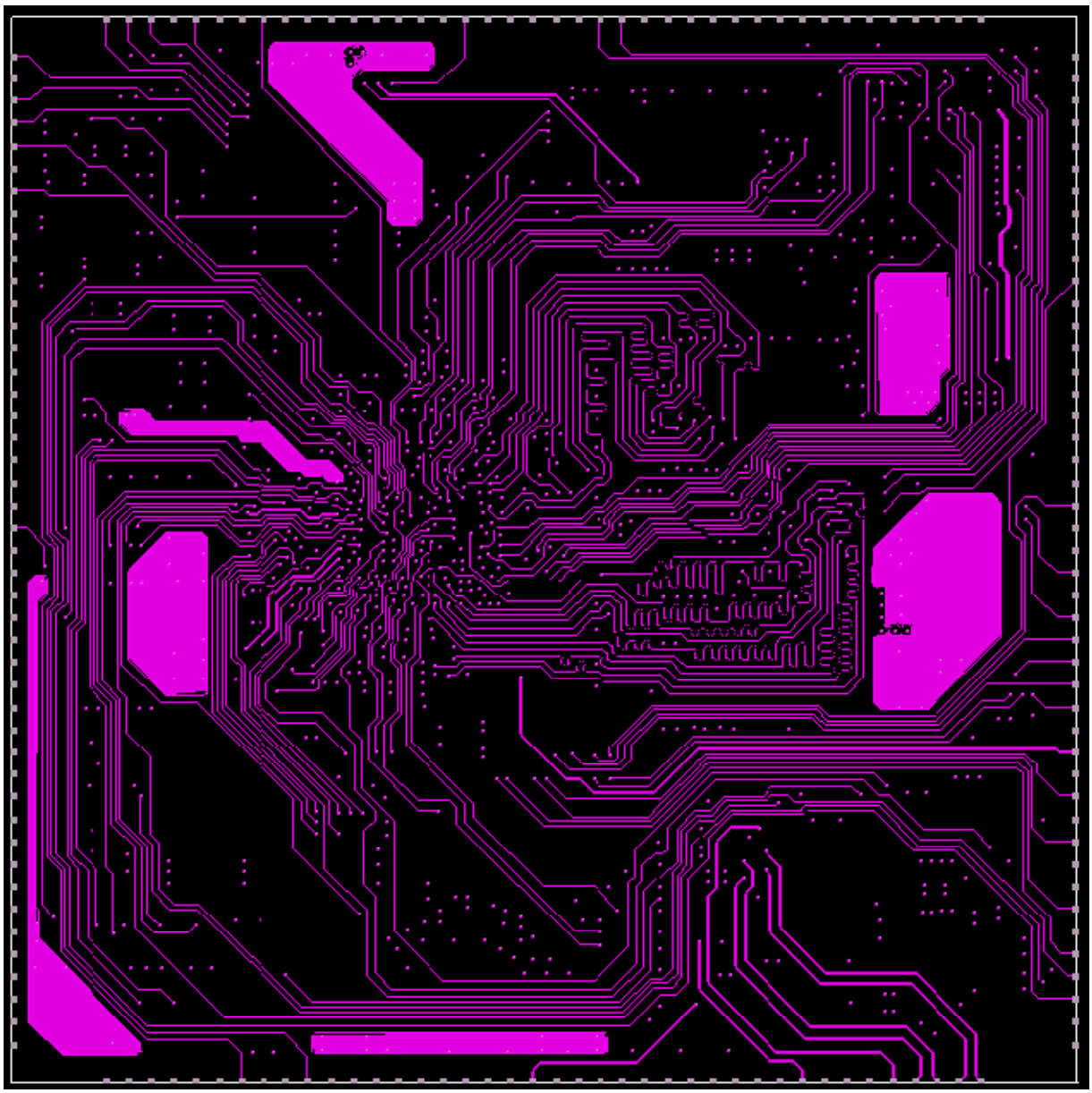


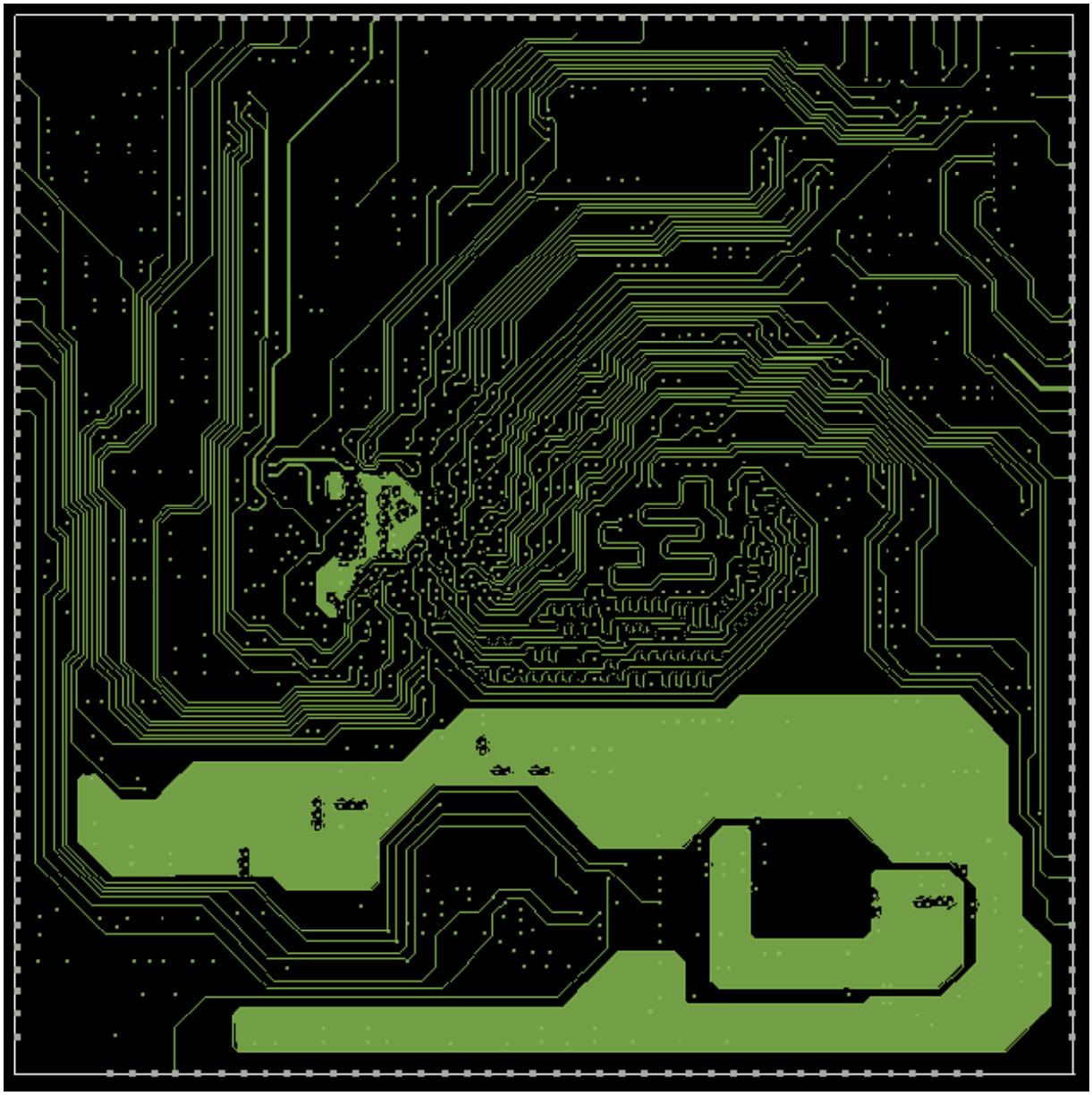
BOARD NAME:CORE6410	LAYERS 8	BOARD THICKNESS 1.0mm+/-10%
UNITS NILS	OPEN WINDOWS:	SPELL MODE:
SOLDER MASK IPC SM-840(COLOR GREEN)		
SILKSCREEN COLOR: WHITE		
DIELECTRIC MATERIAL: FR-4		
Cr@1GHz To INH2 4 2---4 5		
PLATED TECHNICS: [4]	1 HASL(Sn/Pb) 2. HASL(Pb-free) 3. GOLDEN FINGER,OTHERS SPRAYED WITH TIN SOLDER (Pb-free) 4. ENIG 5 OTHERS(ImAg/ImSn/OSP)	
SINGLE IMPEDANCE [Zo]	50+/-10% Ohm with 5mil trace width for layer 1&8 50+/-10% Ohm with 4mil trace width for layer 2&4&5	
DIFF IMPEDANCE [Zo]	100+/-10% Ohm with 5 1/8/5.1 for layer 1 100+/-10% Ohm with 4.1/8/4.1 for layer 2&5	
SHORT NET NO.	SHORT NET POSITION	
[0]		
DESIGN BY EDADOC	QA:002	E-MAIL:NI88@PCBDOC.COM Tel 0755-88852189

3.5 Core board layout

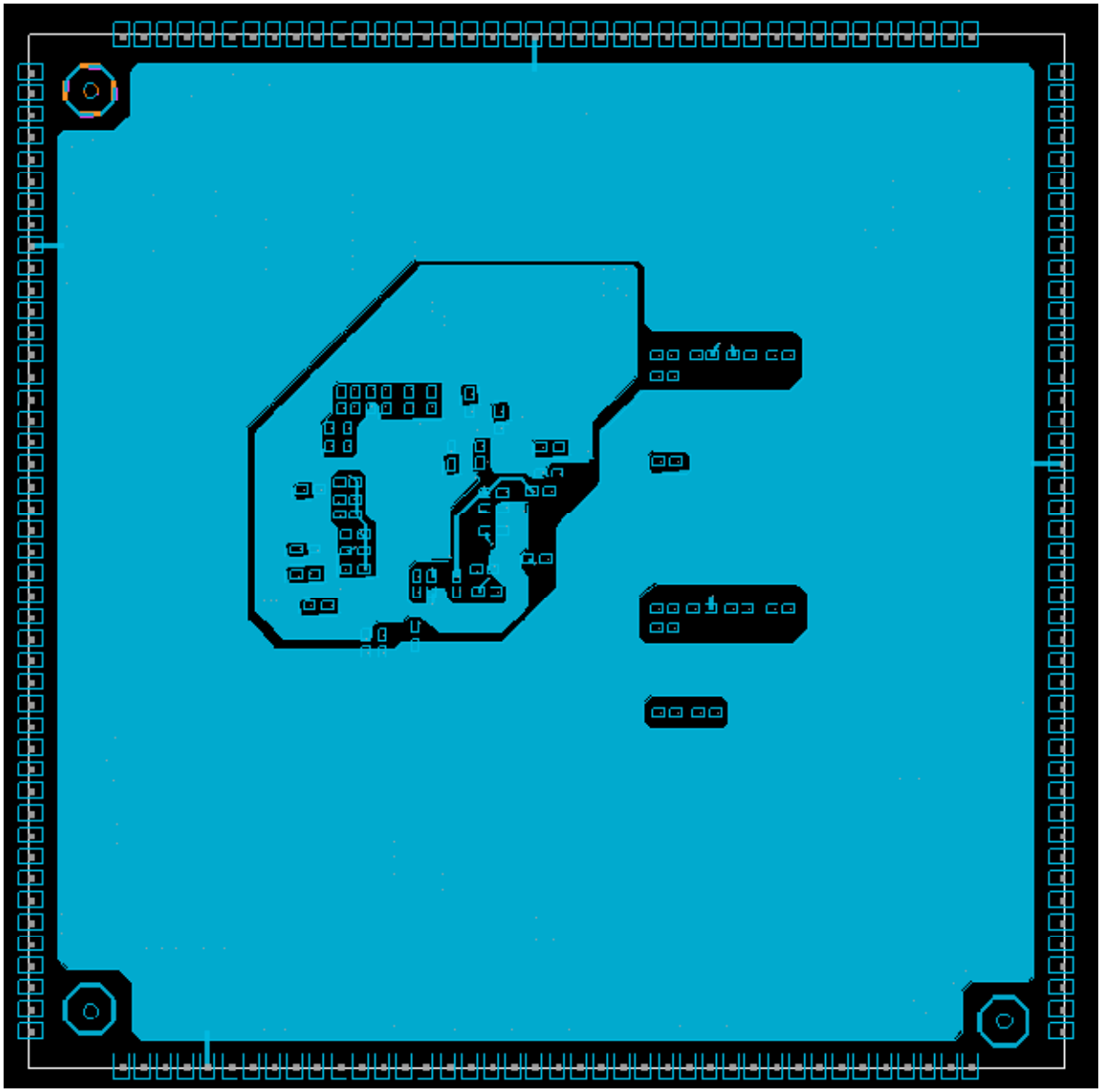








Power plane separation:



Components placement: